Ultra-Broadband GaAs HIFET MMIC PA

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***Abstract* — This paper reports the first MMIC using the HIFET (High-Voltage, High-Impedance FET) concept with very broadband power performance and small die size. This GaAs MMIC power amplifier has a gain of 21dB ± 1dB and over 2W of P_{1dB} over the entire 30 MHz to 2.5 GHz frequency band with 20% efficiency, at a bias voltage of +20V. We believe that this is the first MMIC ever reported which achieves this combination of instantaneous bandwidth, output power, and efficiency, within a die size of 4 mm^2.**

***Index Terms* — High-voltage techniques, Microwave devices, Microwave power FET amplifiers, MMIC power amplifiers, Power amplifiers, Power FETs, Power semiconductor devices.**

I. Introduction

Multi-octave bandwidth power amplifiers are needed for EW, broadband software radio (such as JTRS), and instrumentation applications. The most popular approach to date to achieve such broadband is the Traveling Wave (TW) amplifier configuration. The drawbacks with TW amplifier are that it has relatively low efficiency and that it requires large chip real estate, leading to high price.

Microwave and mm-wave semiconductor devices such as GaAs FET and CMOS usually have sub-micron features and high-doping densities to achieve enough gain at high frequencies, but resulting in low breakdown voltages. Therefore these devices have to be operated at relatively low voltages (< 10V). Consequently, in many applications requiring high voltages, designers try to increase the voltage bias of microwave circuits by connecting several devices DC in series but RF in parallel [1-2]. While connecting devices DC in series helps in biasing at higher voltages, the RF impedance of the RF parallel combination becomes very low, leading to difficulties in matching for broadband applications. Recently, there have been reports [3-6] of high DC bias voltage operation from FET, PHEMT, SiC and GaN devices. But theses devices are either very expensive or still in the R&D stage with immature technology.

In this paper, we report an innovative approach to achieve a high-voltage, broadband, low-cost MMIC PA, with state-of-the-art performance having 21dB gain, 2W output power and 20% efficiency over an instantaneous bandwidth from 30MHz to 2500MHz, with a small chip size of 4 mm^2. We used the High-Voltage/High-Power configuration described in [7] to achieve this performance. We believe this is the first reported on the combination of bandwidth, output power, gain, efficiency and die size.

II. HIFET Configuration

The HIFET configuration is to stack up existing mature device, such as FET, CMOS, or GaN HEMT both DC and RF in series to operate at high voltages and high impedance while acting also as a power combiner. Fig. 1 shows an example of 4 identical FETs connected in series in HIFET configuration. The positive drain bias is applied to top FET4. But the negative gate bias is applied only to bottom FET1. The shunt resistors are designed for RF feedback as well as to ensure that the gate-to-source bias of FET2, FET3 and FET4 are the same as FET1 , such that all FETs have the same drain-to-source voltage. The RF input is only applied to bottom FET1, and the RF output is from top FET4. This arrangement has the advantage of improving the HIFET amplification gain over the individual FET gain because the RF input is only applied to FET1, yet the RF is from the drain of FET4, which is the total power of HIFET.

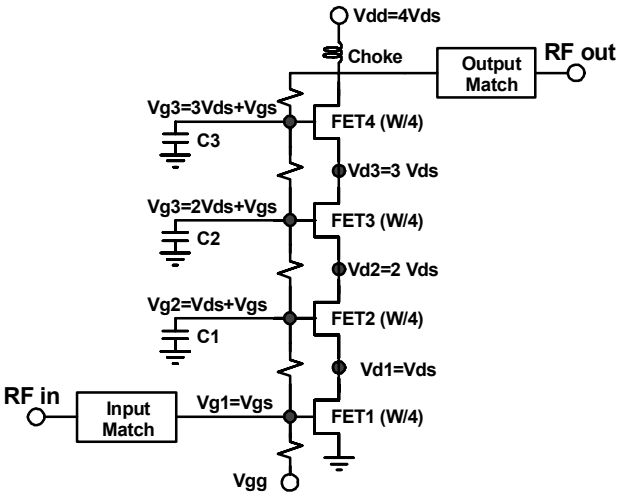

Fig. 1. HIFET configuration, with both DC and RF in series.

Table I illustrates the advantages of using the HIFET. The major advantages are: a). High DC bias voltage b) High RF impedance, which leads to broadband capability and high power, and c) A bonus gain of $10\text{Log}_{10}(N)$ dB over the individual FET gain, which leads to high frequency capability (N is the number of FET in series).

There are three important criteria to meet for the HIFET to operate properly: a) Each FET cell needs to have the same gate-to-source bias, which is a pre-requisite for series operation. b) Each FET cell should see the optimal impedance to deliver the best possible output power and efficiency. And c) The RF voltage of each FET cells should have the same phase so the power of each FET cells adds to achieve the best output power and efficiency. These criteria can be achieved by the proper choice of the resistor and capacitor values in Fig. 1.

TABLE I: COMPARISON BETWEEN TRADITIONAL (PARALLEL) POWER COMBINER & HIFET CONFIGURATION

Parameter	Parallel Configuration	HIFET Configuration
Drain Voltage	V_d	N x V_d
Drain Current	N x I_d	I_d
Input Impedance	Z_{in}/N	Z_{in}
Output Impedance	Z_{out}/N	N x Z_{out}
Gain (dB)	G	G + 10Log$_{10}$ N
Output Power (dBm)	P	P + 10Log$_{10}$ N

This paper describes the development of a broadband MMIC, taking advantage of this new device configuration to achieve state-of-the-art high power, high efficiency, and broadband performance with a very small die size.

III. MMIC DESIGN

To illustrate the HIFET principle, we will use a simple low frequency model for easy understanding. Power devices deliver an amount of power proportional to the device total gate periphery. Power devices should also be matched to their optimum load impedance to deliver the maximum power. This impedance is inversely proportional to the device gate periphery, which poses real challenges to a designer trying to achieve high power and broadband performance. The optimum load impedance Z_{opt} of a regular FET at low frequency (i.e. ignoring capacitance effects) is equal to

$$Z_{opt} = (V_{ds}-V_{knee})/I_{ds} . \quad (1)$$

V_{ds} is the drain voltage
V_{knee} is the device knee voltage of the I-V characteristics
I_{ds} is the operating current

As the device size increases, the bias current also increases proportionally resulting in very small value of the optimum impedance. Small optimum impedance is very difficult to match to 50 Ohms without excessive matching circuit loss, particularly over broad bandwidths. Moreover complex matching networks can take a lot of valuable semiconductor real estate, resulting in large die size.

In order to achieve ultra broadband amplification, one of the best approaches is to tailor the device impedance to be 50 ohms. In this case, no impedance matching is needed. Because the HIFET optimal impedance is the sum of individual FET cell impedance, it is possible to choose the FET cell periphery and the number of the cells in series to achieve 50-ohm load impedance. This is the main design criterion of the broadband MMIC in this paper.

The optimum impedance Z_{opt} of a HIFET consisting of N cells in series is

$$Z_{opt} = N(V_{ds}-V_{knee})/I_{ds} . \quad (2)$$

The MMIC described in this paper is a 2-stage design with 4 FETs in series each for the driver and power stage. The FET cell in the driver stage and power stage are 2mm and 3.6mm respectively. The 3.6mm FET has I_{dsss} = 0.72A, V_{ds} = 5V, V_{knee} = 0.5V. Therefore using (2) and assuming I_{ds} = 0.5 I_{dss} = 0.36A, the 4 x 3.6mm power stage HIFET optimal load impedance is near 50 ohms. Fig. 2 shows the MMIC circuit diagram.

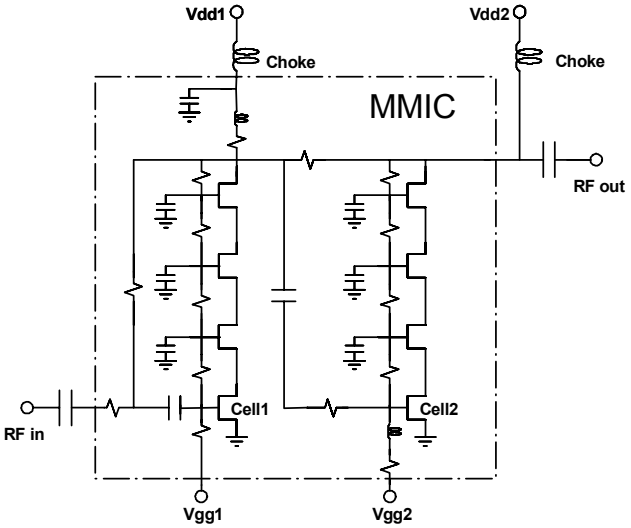

Fig.2. MMIC circuit schematic diagram.

Because the output optimal load impedance is near 50 ohms, no output matching circuit is needed. The inter-stage matching is a simple R-C circuit. The input matching to the driver stage is accomplished using a simple combination of resistive matching and resistive feedback to achieve ultra-broad bandwidth response. These are key factors in achieving a small die size of 4mm^2.

The driver stage gate is biased through a large resistor to achieve broadband matching by reducing the gain roll-off at low frequency end. The HIFET device feedback resistors and compensating capacitors are integrated within the MMIC. The DC blocking capacitors at the input and output RF ports need to have large values (>1000pF) to extend the bandwidth down to 30MHz and are kept off-chip as shown in Fig. 2. The drain of the power stage is biased thru the output RF port using a bias-tee. The HIFET is potentially unstable, however the combination of resistive matching and resistive feedback made the MMIC stable from DC to 20GHz as shown in Fig. 3. The stability factor K is greater than 1 and the B1 factor is positive for all the frequencies.

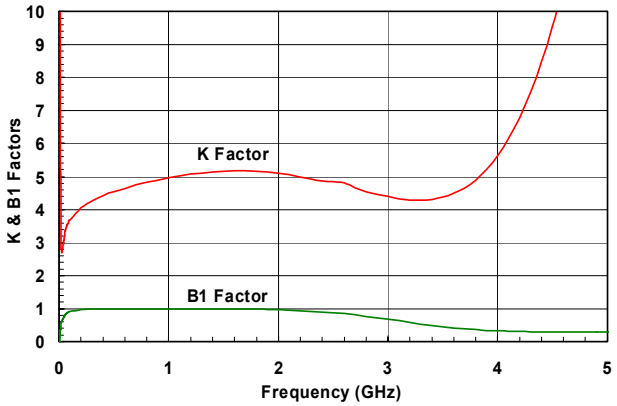

Fig. 3. MMIC PA stability factor

IV. MMIC Fabrication

The MESFET foundry process uses the standard M/A COM 0.5µm gate-length, single-recess process with typical drain-to-gate breakdown > 13V. Typical power density from this process is 0.3W/mm at 5V operation. The MMIC design uses thin film Tantalum Nitride resistors and epitaxial resistors. Capacitors use 1500°A thick Silicon Nitride dielectric.

Fig. 4 shows the photograph of the MMIC. The input stage is a four 2mm-FET HIFET. The output stage consists of 2x 4 1.8mm HIFET in parallel. The chip size is very small, 2.23 x 1.82 x 0.1 mm, because there is no output matching circuit needed. In this compact size all matching is on-chip except the DC-blocking capacitors at the input and output RF ports and the bias circuits of the driver and power stages. The MMIC is packaged in a low cost SMT ceramic package having a size of 0.25 x 0.25 inch^2. The MMIC is AuSn eutectically attached to the package copper base for low thermal resistance.

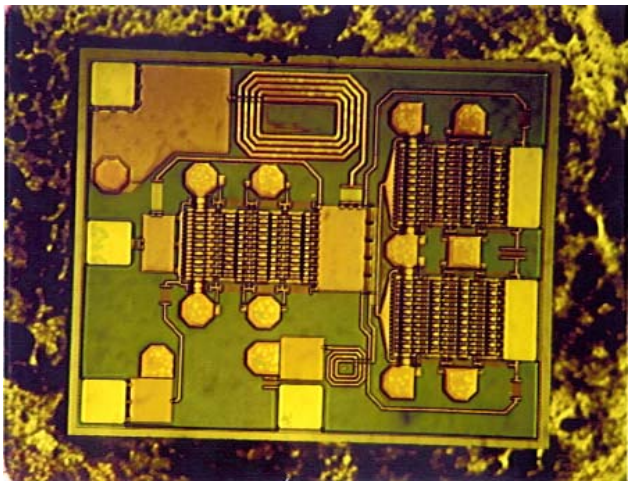

Fig. 4. MMIC chip photograph.

Fig. 5 shows a photo of the packaged MMIC. The MMIC was tested on a PC board made of 10-mil FR4 material. Multiple vias on the PC board are used under the SMT package to keep the thermal resistance of the PC board as low as possible as well as to provide low impedance to ground.

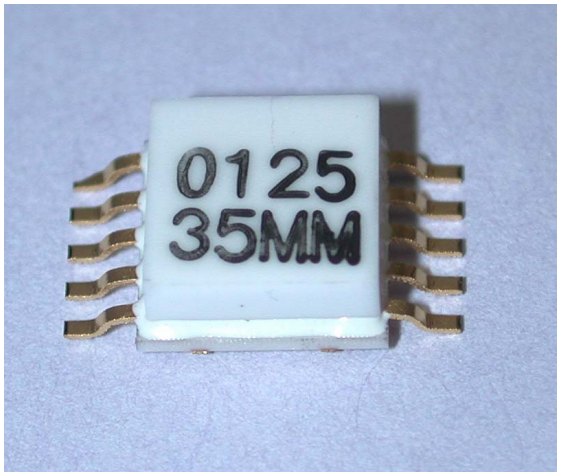

Fig. 5. Photograph of SMT package.

V. MMIC Performance

The packaged MMIC was tested using an external bias tee. The test results include the losses of the test fixture which are a few tenth of a dB. Fig. 6 shows the measured and simulated small signal gain of the MMIC. The gain is 21dB ± 1dB from 30MHz to 2.5GHz. As shown in Figure 6, the simulated gain agrees well with the measured gain, indicating the accuracy of our model. The input return loss is > 15dB. The output return loss is around 15dB up to 2GHz.

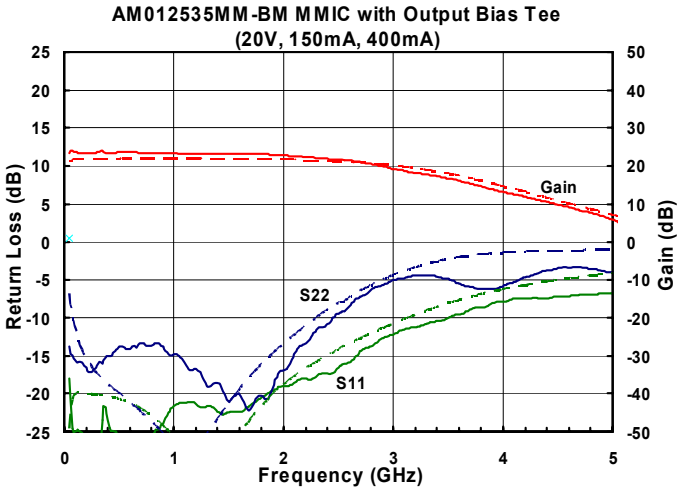

Fig. 6. Small signal measurements & simulation (dashed).

Figs. 7 and 8 show the measured P_{1dB} and P_{sat} versus frequency at +20V bias, respectively. The P_{1dB} is 34 ± 1dBm and the efficiency is > 26% for frequencies below 1GHz and gradually drops to near 20% at 2.5GHz.The P_{sat} is about 0.5dBm over P_{1dB}, and the IP3 in Fig. 9 is 10dB above P_{1dB},

indicating that the MMIC PA is fairly linear. This good linearity is attributed partially to the negative feedback used in the HIFET configuration. We believe this combination of output power, efficiency, gain, bandwidth and die size is the best reported to date.

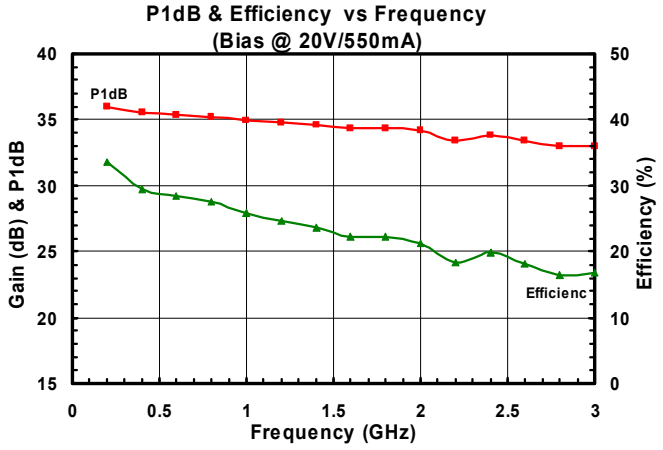

Fig. 7. P_{1dB} & efficiency versus frequency.

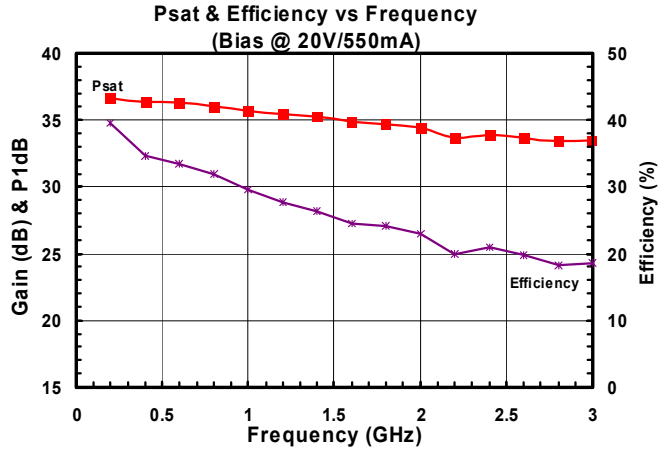

Fig. 8. Saturated power & efficiency versus frequency.

V. Conclusion

This paper describes the first ultra broadband GaAs FET MMIC PA design using the HIFET configuration with state-of-the-art performance. The results demonstrate the potential of the HIFET configuration for achieving simultaneous broadband, high-power, high-voltage, high-efficiency and small die size, which can have numerous RF and microwave applications, such as EW, broadband software radio and instrumentation. Although this paper is based on the GaAs FET MMIC, the HIFET concept is not limited to GaAs technology. The concept can easily be applied to other semiconductor technologies such as CMOS (Such as for WLAN and WiMAX) to overcome low voltage operation, or to GaN, SiC and other Silicon devices to deliver very high power.

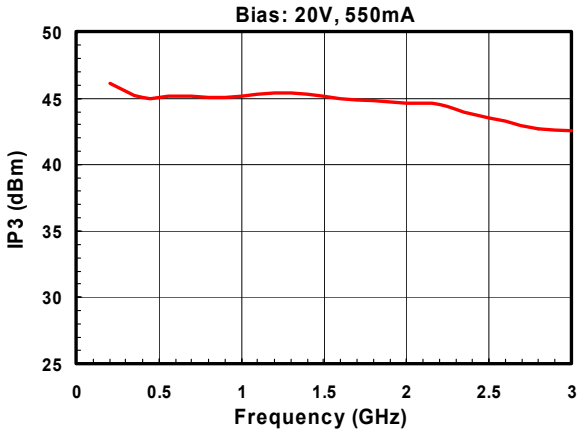

Fig. 9. IP3 versus frequency.

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