CMOS PA For Wireless Applications[1]

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[1]This work is partially supported by DARPA, contract No. N66001-04-C-8034

AMCOM COMMUNICATIONS
The RF Power House

IEEE

Presentation Outline

- Why do we need a CMOS high-voltage device?
- Brief description of the HIFET configuration
- 0.18μm Low-voltage operation CMOS process description & HIFET device design
- RF data results of HiFET CMOS
- Conclusion

Why High Voltage Device?

- Mitigate low breakdown, low bias voltage in semiconductors devices such as: GaAs FET, pHEMT, InP, sub-micron CMOS.
- Simpler matching for high-power applications
- Higher power and broadband matching
- Some applications require high voltage

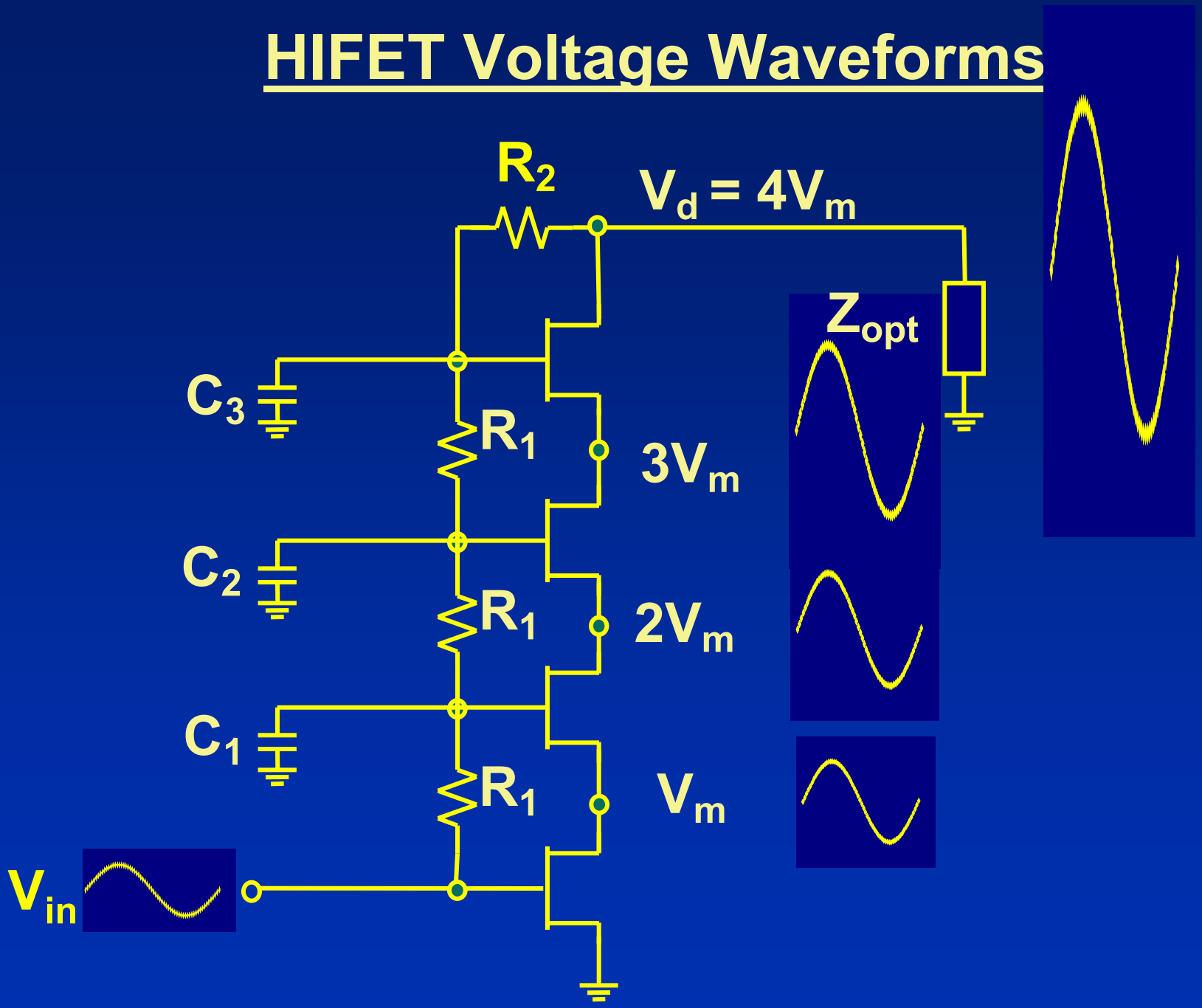
Motivation for Current Work

- Efforts are currently being directed towards integrating the RF PA with TX/RX and BB circuits
- BiCMOS process is a preferred process for integration
- CMOS devices are difficult to match for any significant amount of power
- Si substrate RF losses are significant

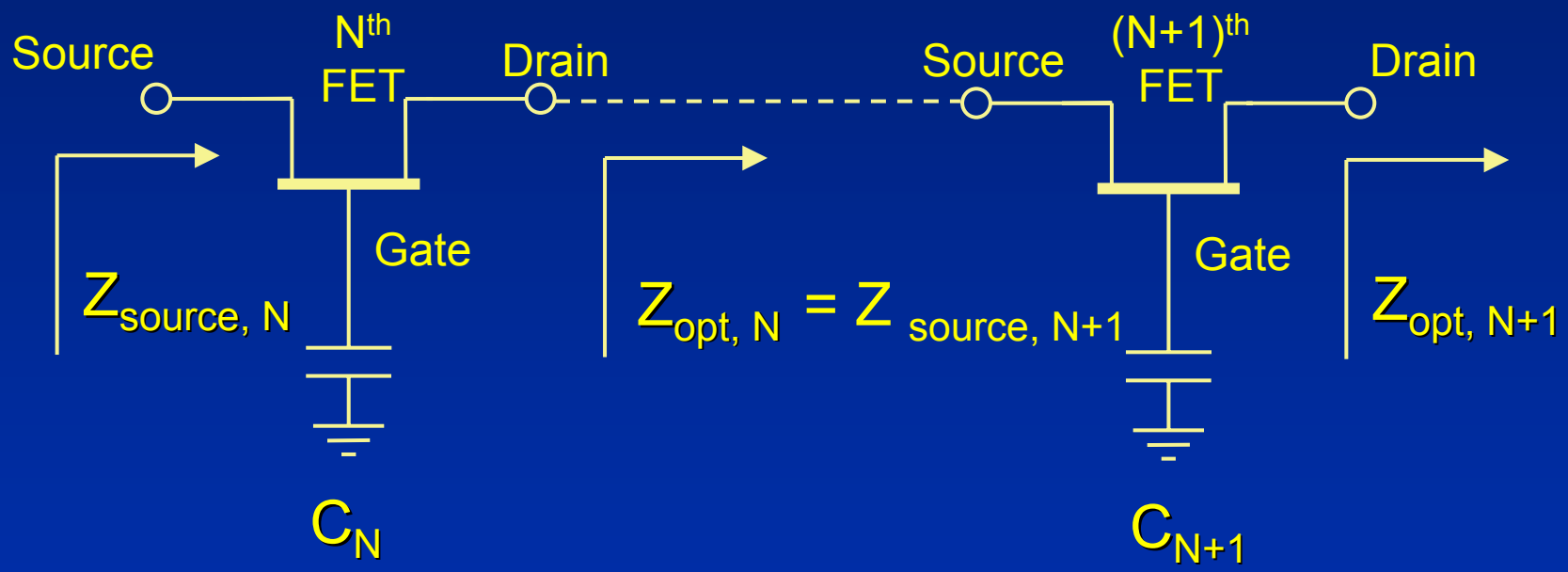
What is HIFET?

- HIFET is an innovative power combining technique connecting identical FETs RF & DC in series.
- HIFET has high voltage and high impedance.
- Output impedance could be raised to near 50Ω.
- HIFET enjoys a bonus gain of 10 Log N dB.
- HIFET concept applies to any FET device such as MESFET, HEMT, CMOS, LDMOS, GaN, SiC etc.

HIFET Voltage Waveforms



Impedance Optimization of Common Gate FET



$Z_{source,\,N} \cong 1/g_m \ (C_{gs} + C_N) / C_N$

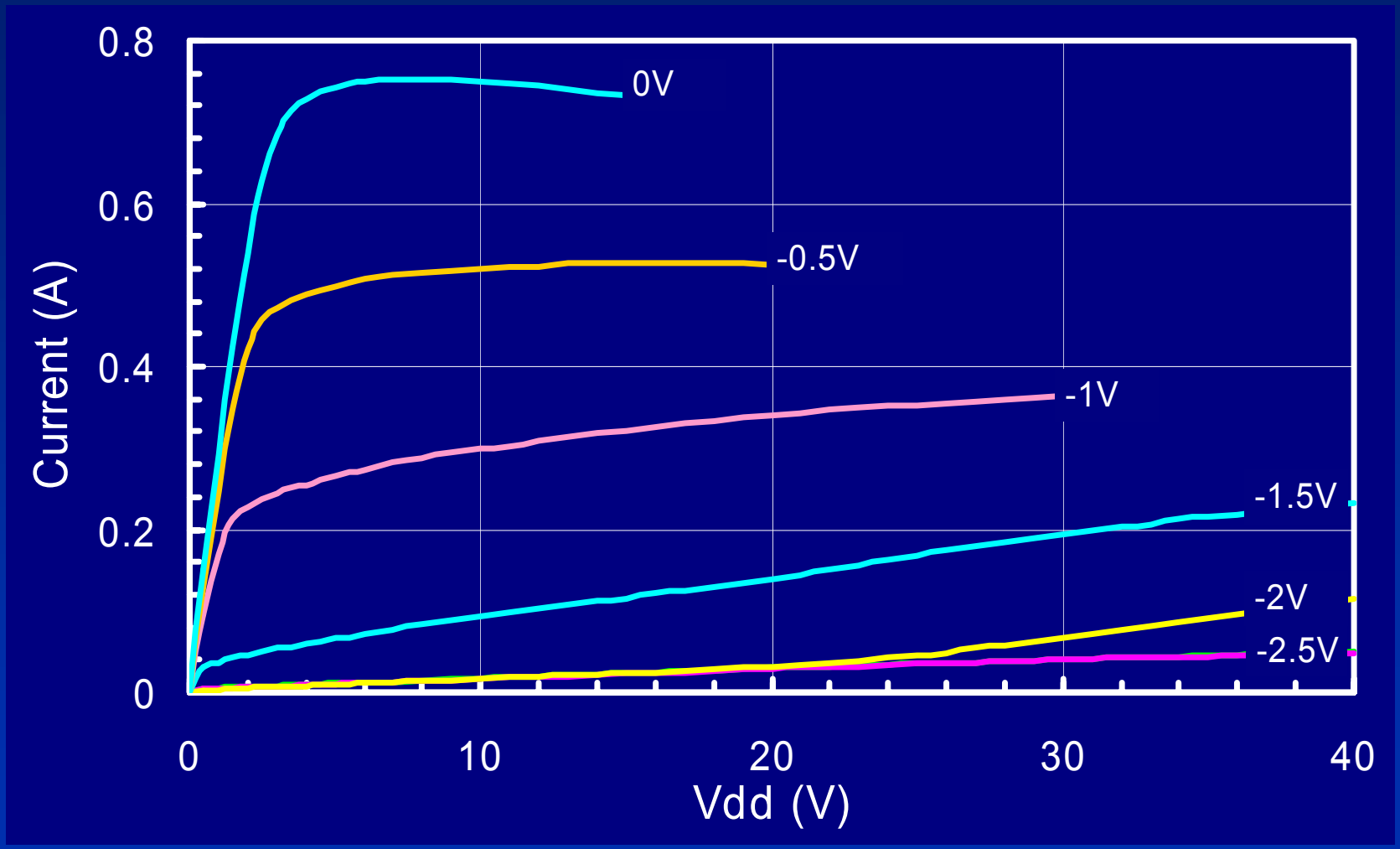
g_m is FET transconductance

C_{gs} is FET gate-to-source capacitance

HiHET Configuration Features

- Equivalent performance to a single device with high voltage (i.e. Ideal power combiner)
- High voltage bias: $V_{dd} = V_{ds} \times N$
- Lower Current by 1/N factor compared to regular FET with equivalent periphery. (i.e. Scaled I-V characteristics)
- Higher optimum output impedance by N^2 factor
- Higher input impedance
- Higher gain by factor of N
- Broadband matching
- Simple & compact configuration
- Concept applicable to any FET technology

I-V Characteristics of a 4 x 3mm GaAs MESFET HIFET



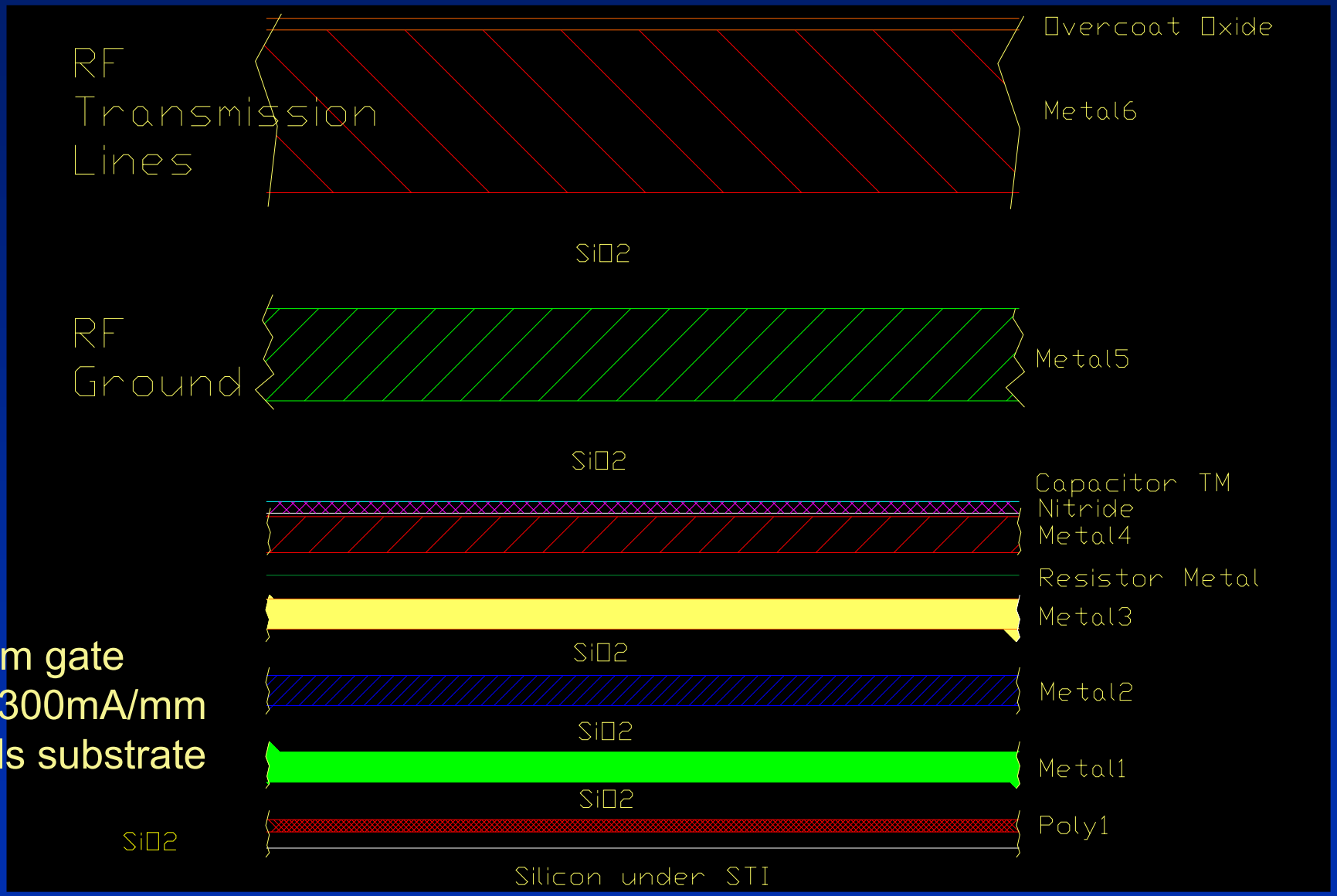
HIFET Device Design

- We have 2 degrees of freedom: N & I_{ds} (Device size)
  - Select a proper cell size
  - Select No. of devices in series
- $R_{opt} = N .(V_{ds}-V_{knee}) / I_{ds}$
- $Pout = N . (V_{ds}-V_{knee}) . I_{ds}/ 2 = N^2 . (V_{ds}-V_{knee})^2/ 2 R_{opt}$
- Design bias & RF feedback resistors for gain flatness, good input & output VSWR and stability
- Adjust capacitor values for optimum power at frequency of operation
- Air voltage breakdown design rule (~ 0.8 to 3V/μm)

HIFET CMOS Process Details

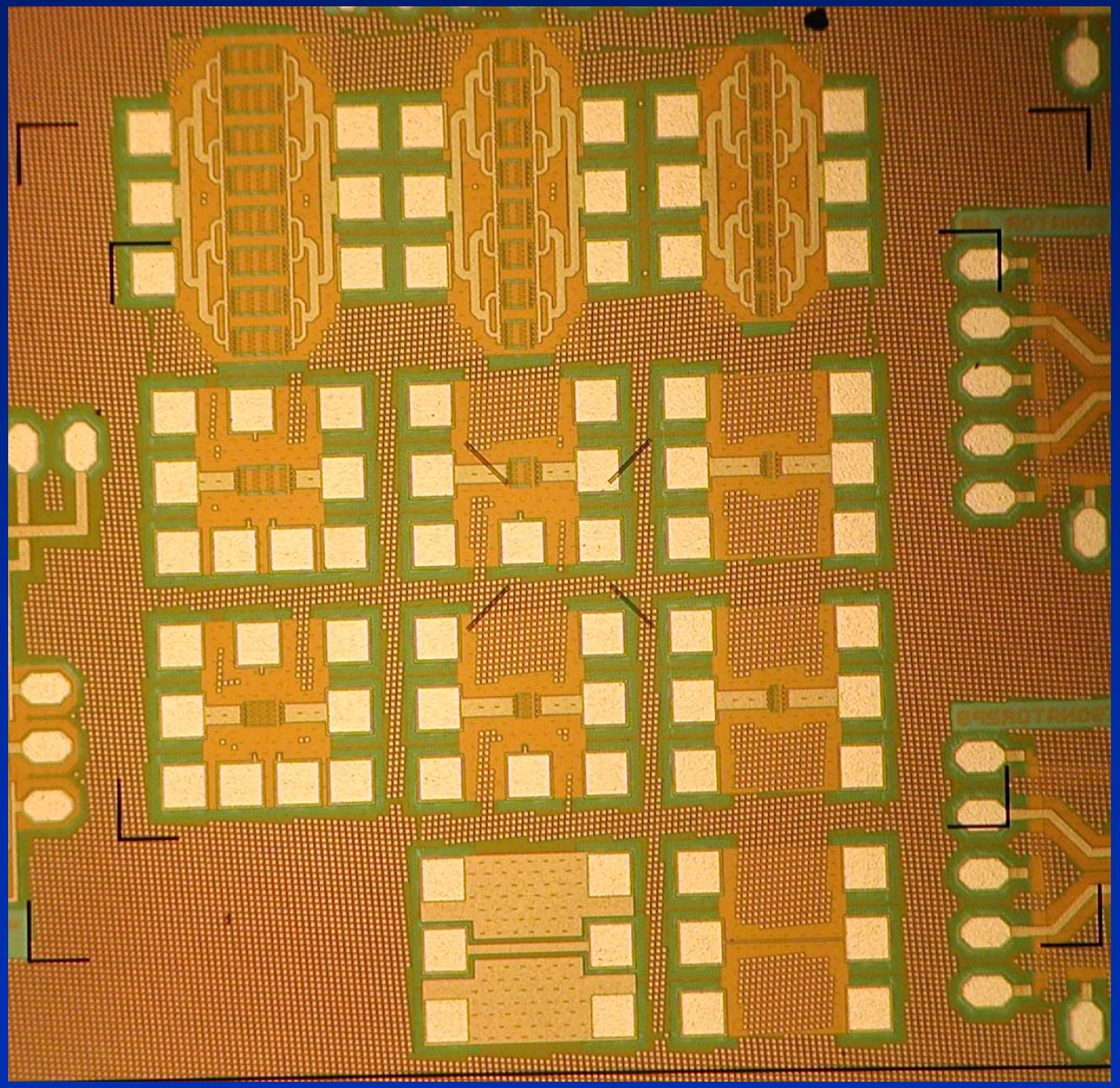
- 0.18μm gate length
- Use thick metals for microstrip lines and RF ground.
- Dielectric for RF lines is 2μm SiO_2
- Silicon Nitride layer for capacitor dielectric
- Implanted n-type resistors (890 Ohms/sq.)
- Thin film resistors
- Basic cell consists of 8 x 10μm
- HiFET: 2 in-series & 4 in-series: 2 x 80μm, 4 x 80μm, 2 x 640μm, 4 x 640μm

CMOS Process Outline

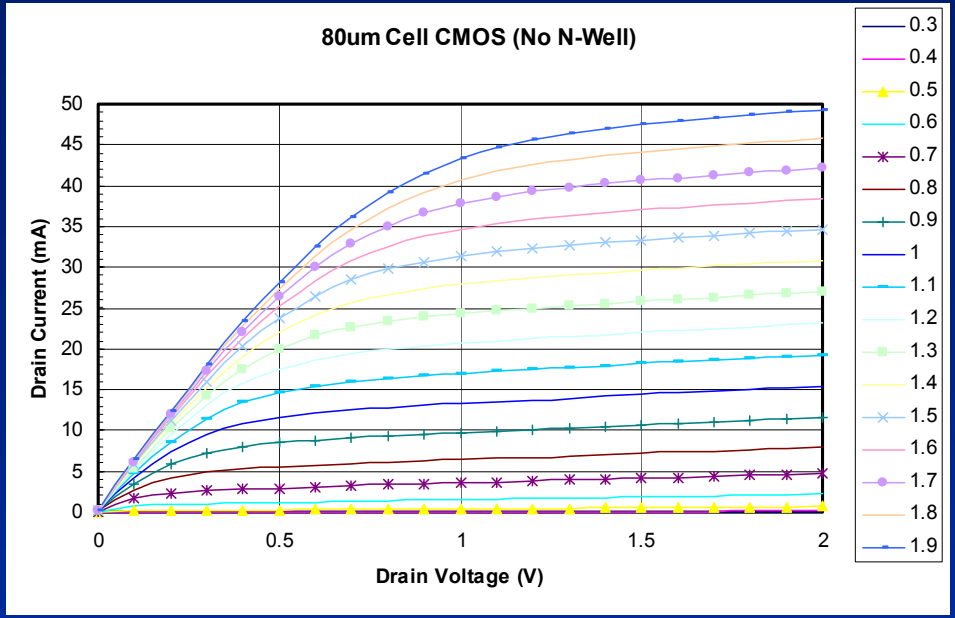


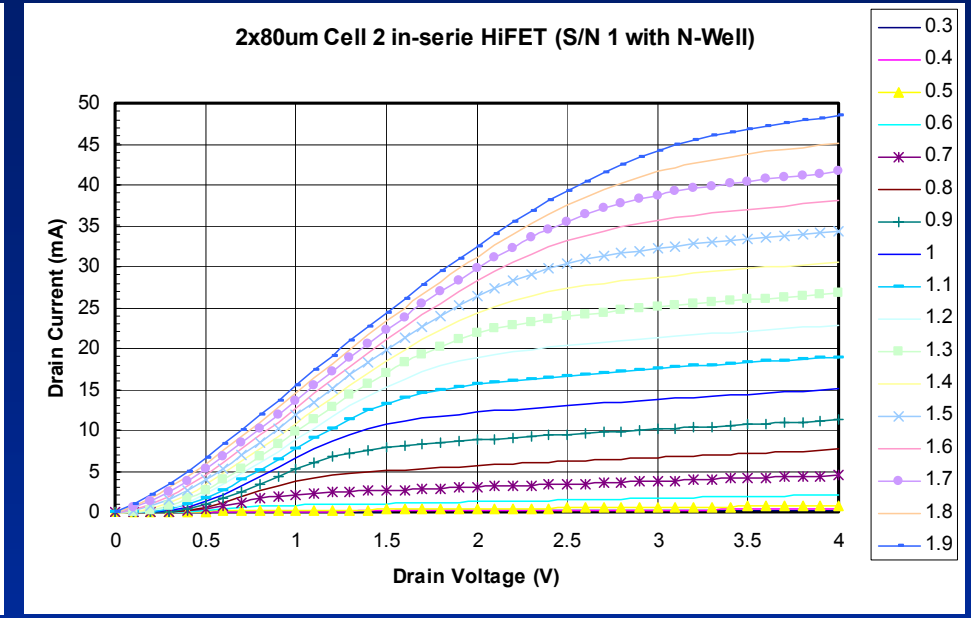
0.18µm gate
Ids ~ 300mA/mm
10 mils substrate

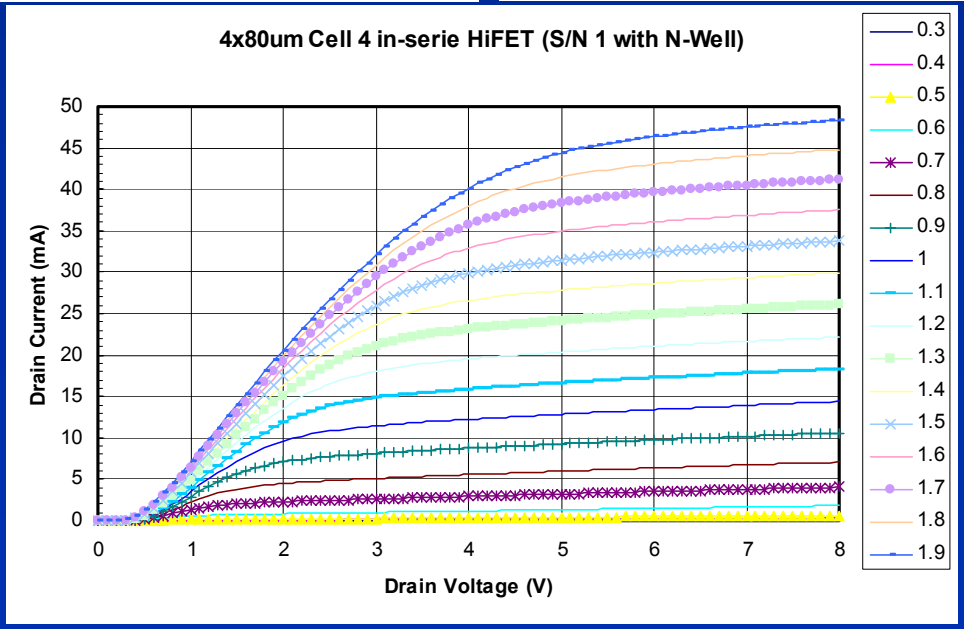
Picture of Fabricated Test Circuits



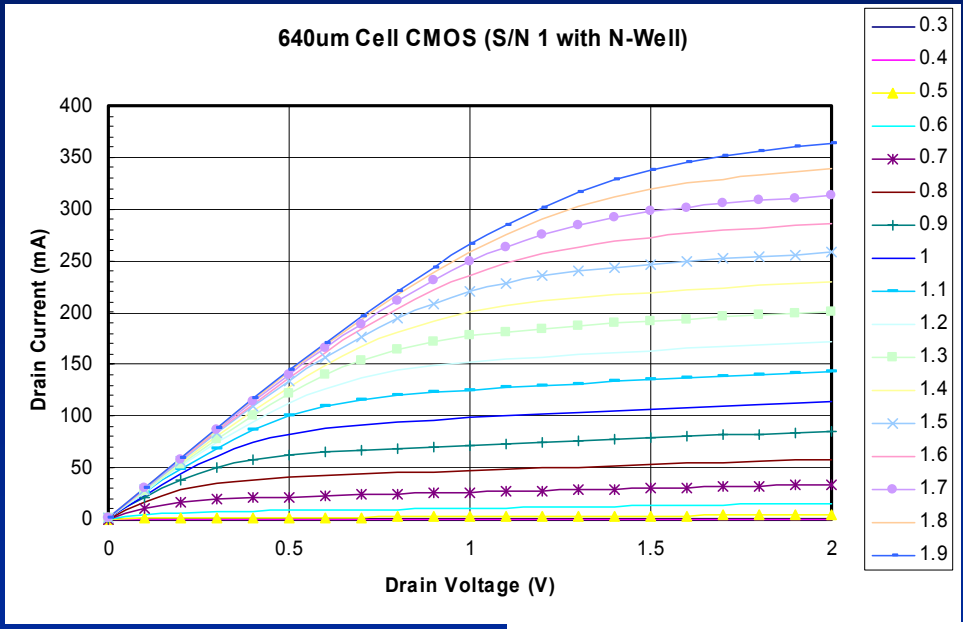
I-V Characteristics of a 80µm Single Cell, 2 in-series & 4 in-series

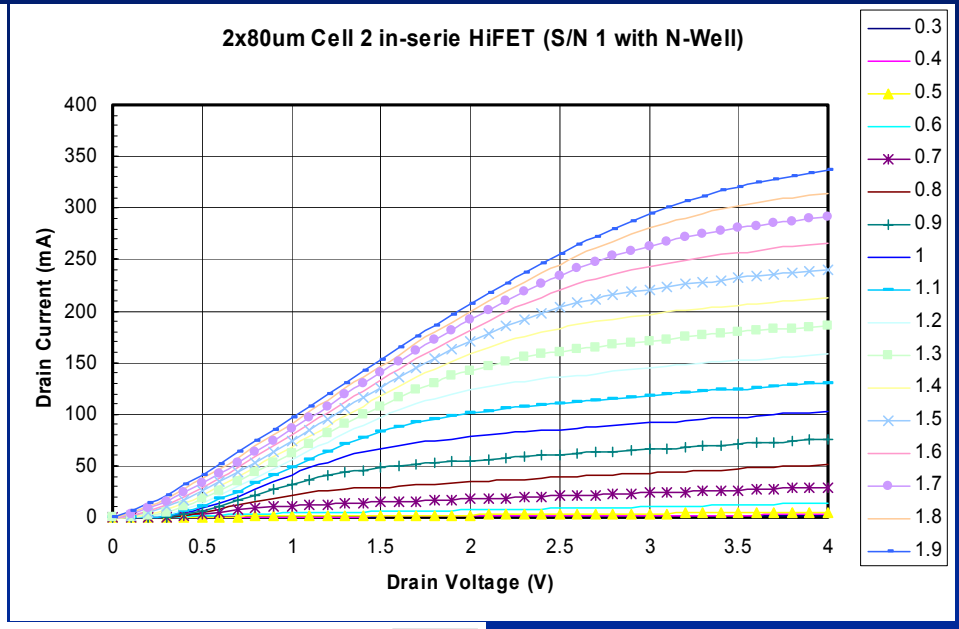


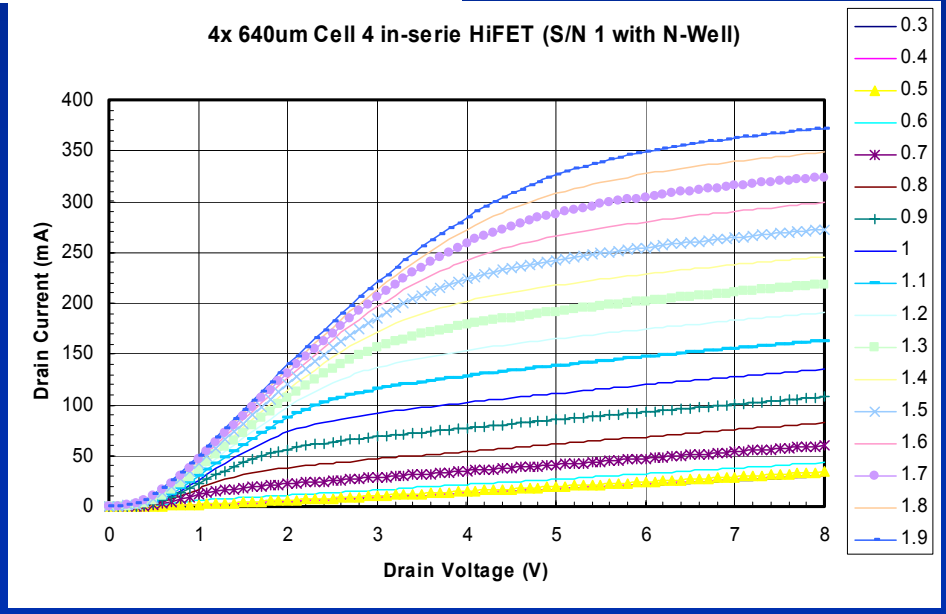




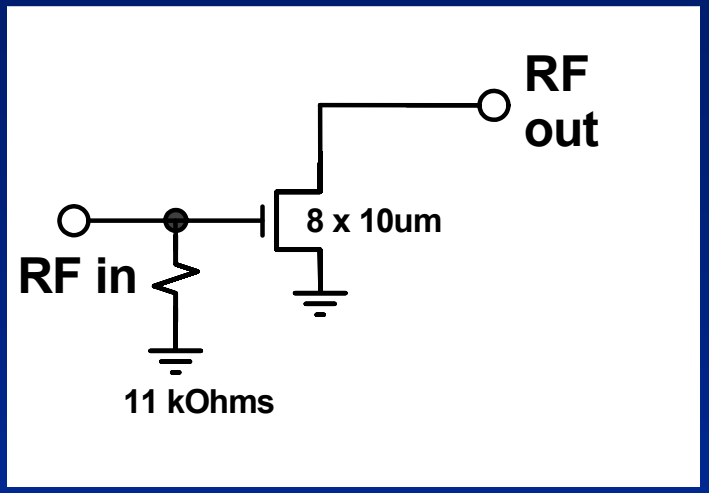
I-V Characteristics of a 640µm Single Cell, 2 in-series & 4 in-series

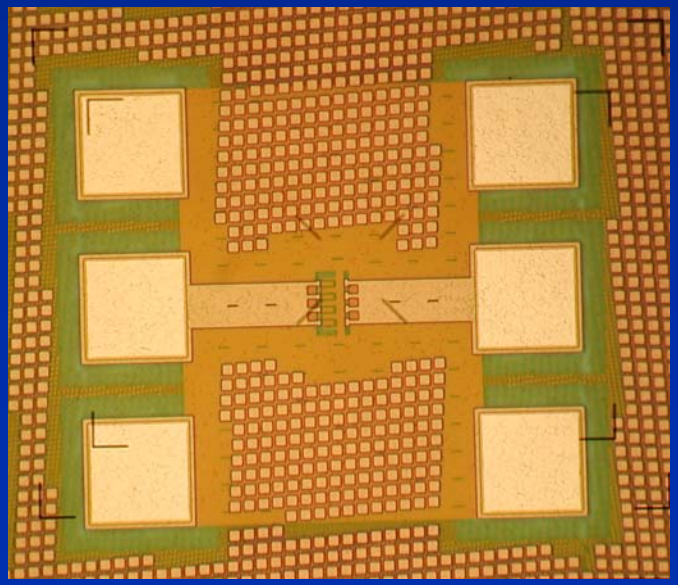


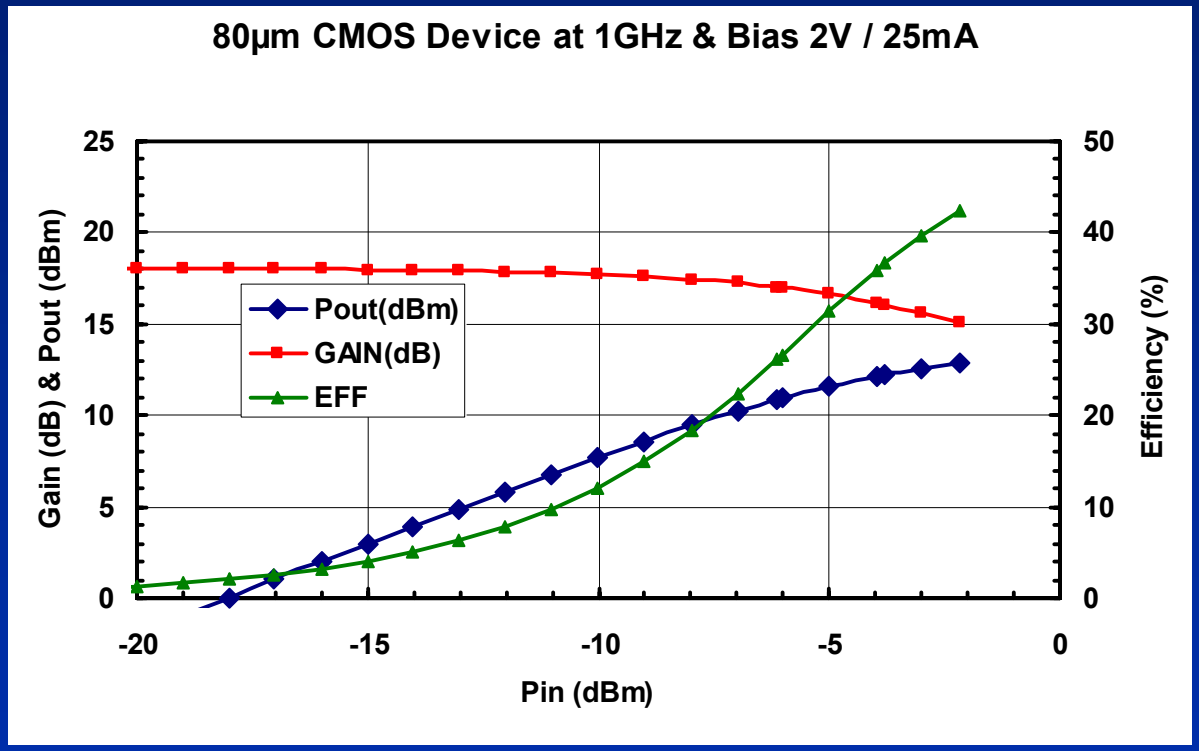




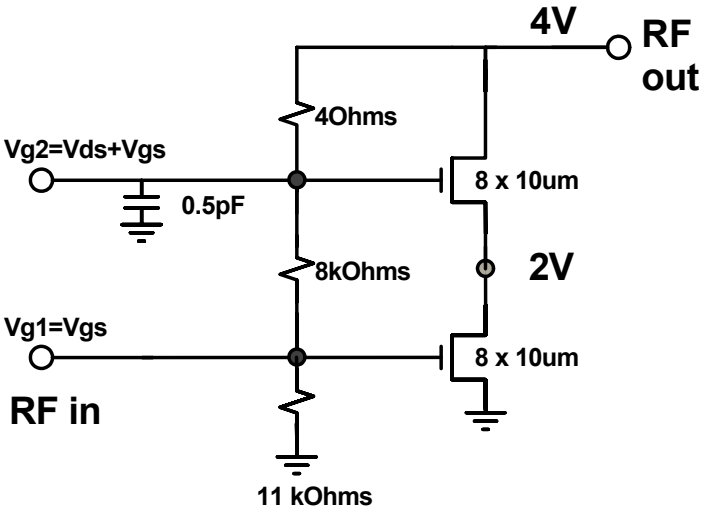
Power of 80µm Cell at 1GHz

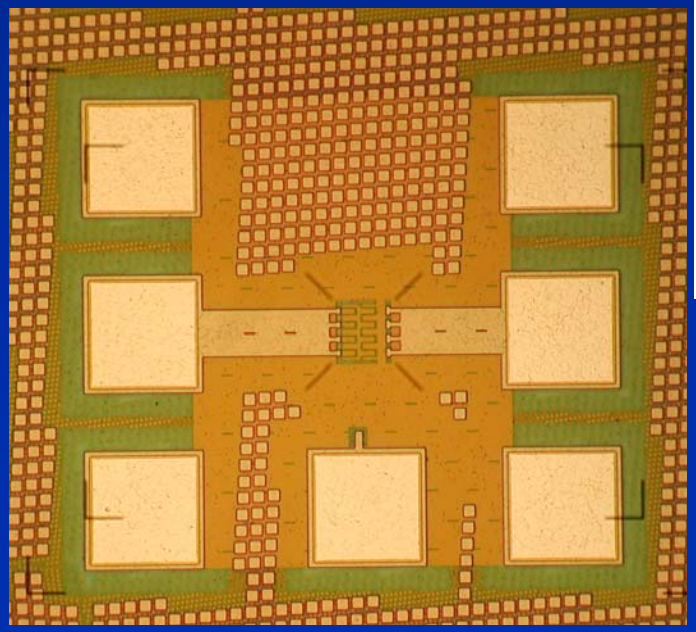


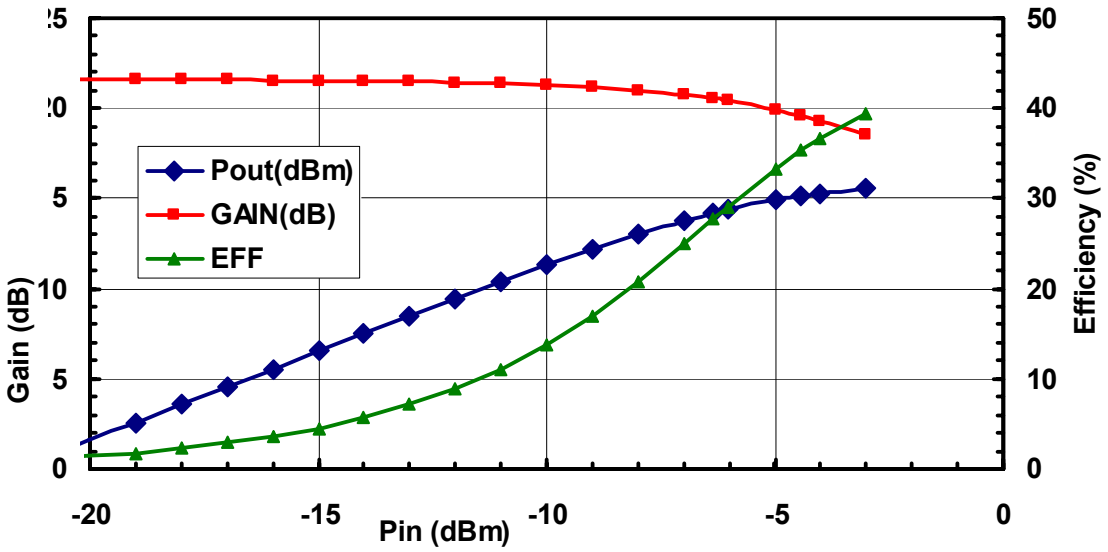




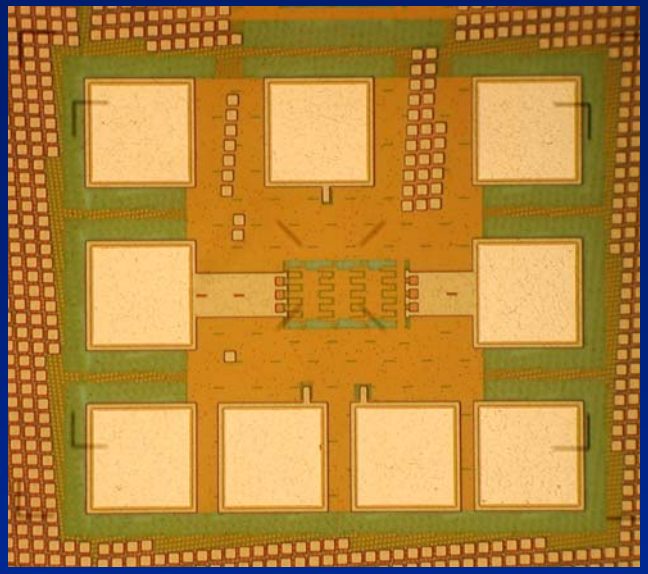
Power of 2 x 80µm HiFET at 1GHz

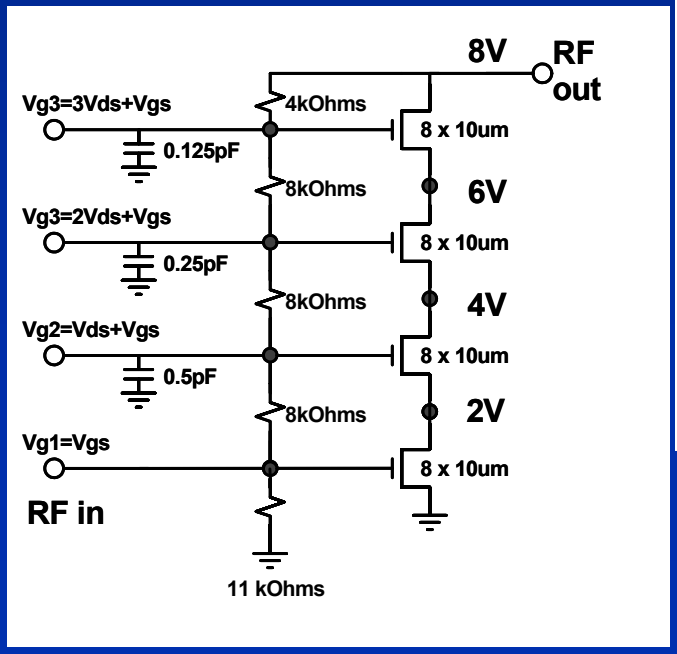


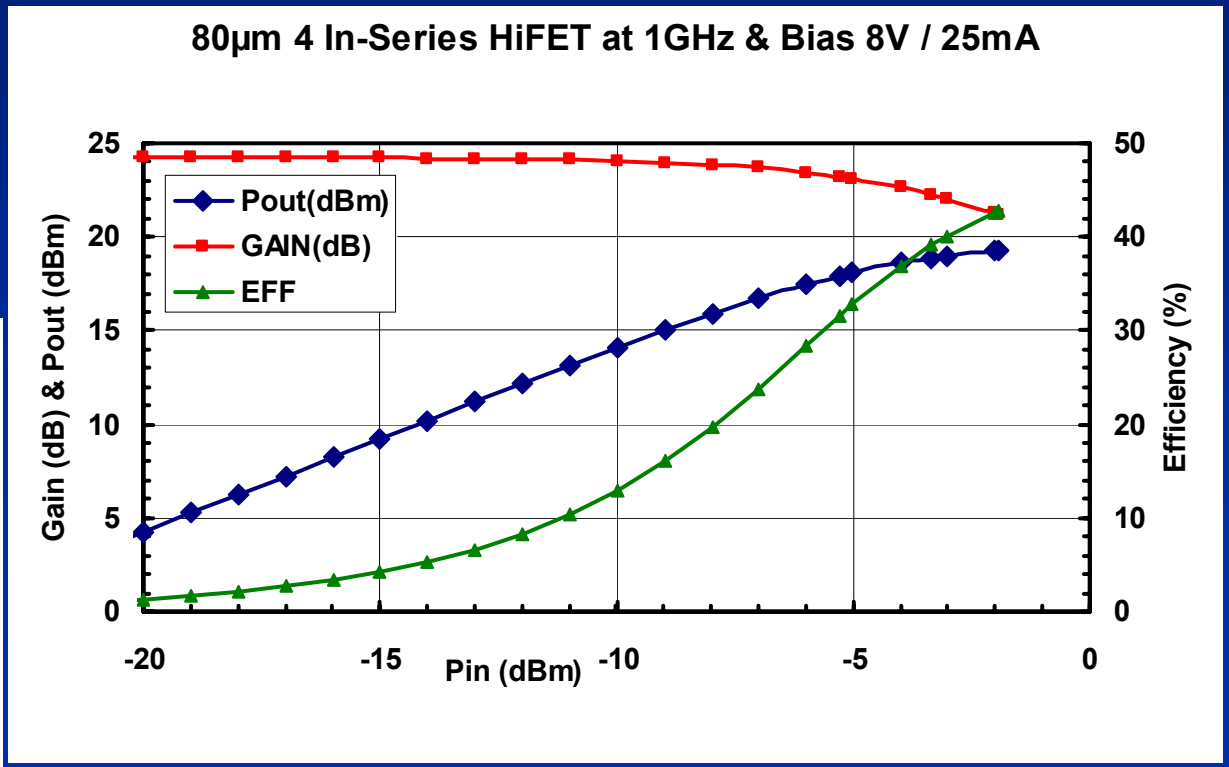




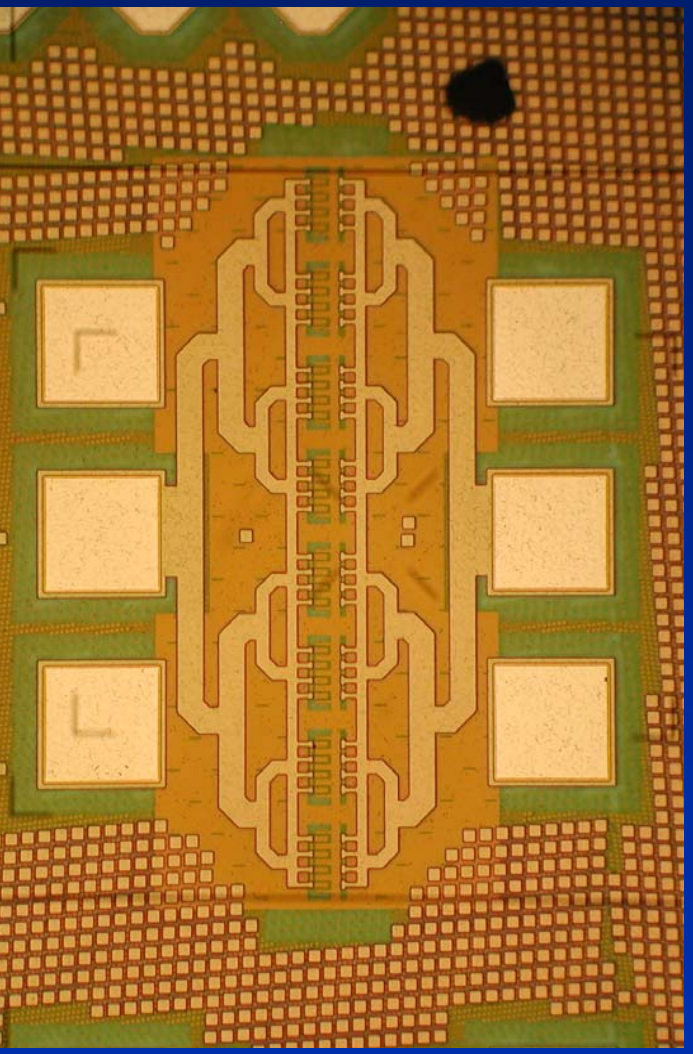
Power of 4 x 80µm HiFET at 1GHz

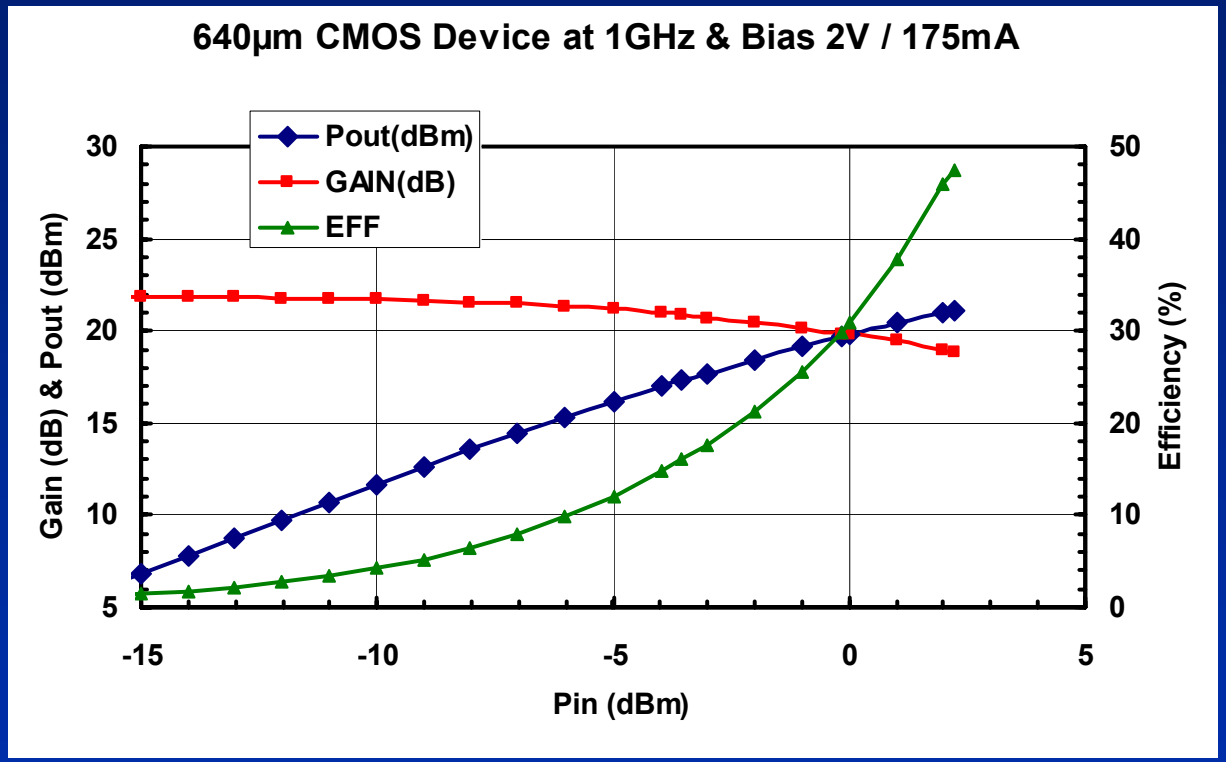






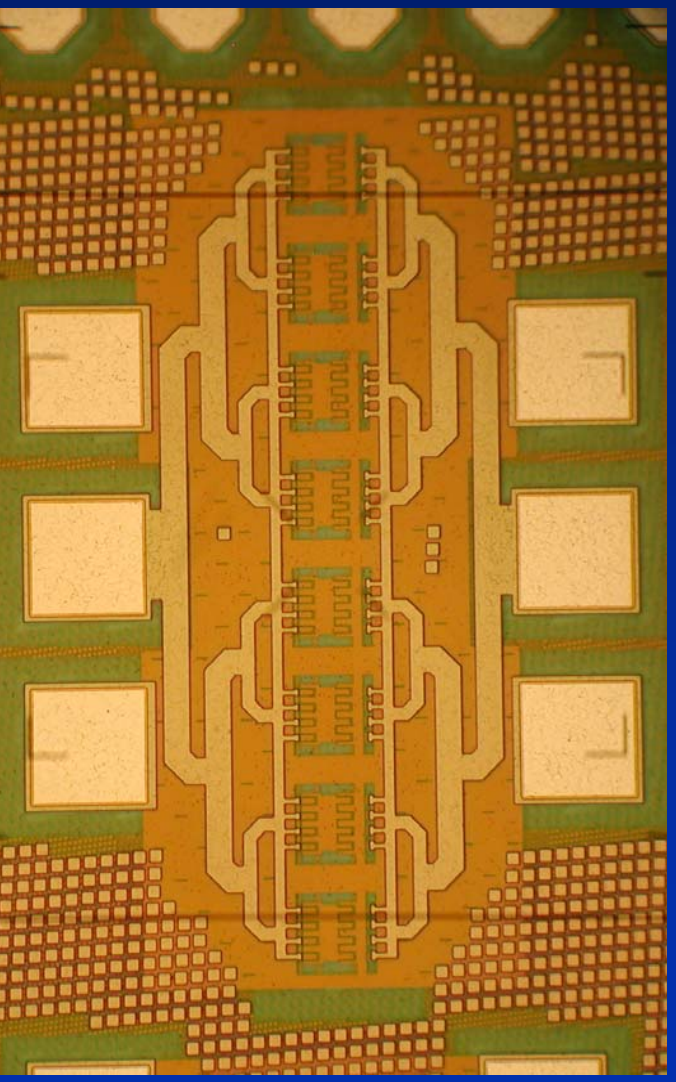
Power of 640µm Cell at 1GHz

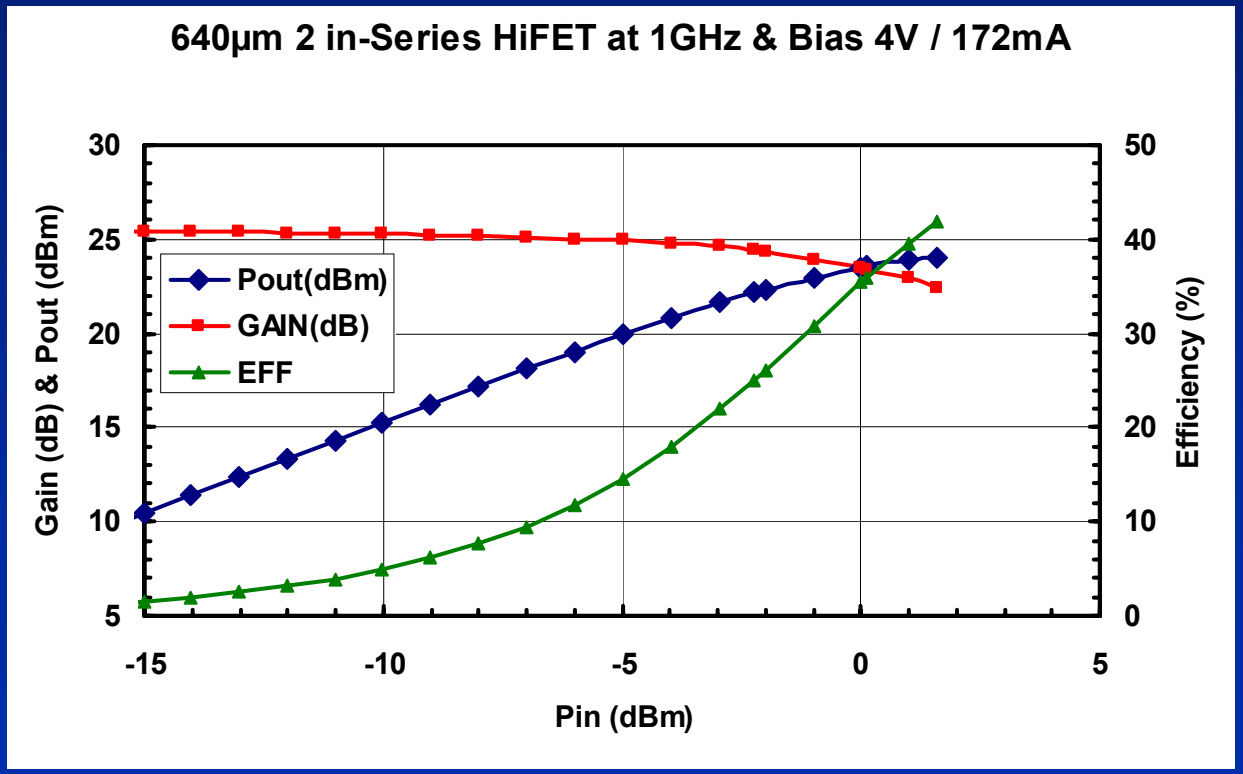




R_{opt}= 10 Ω

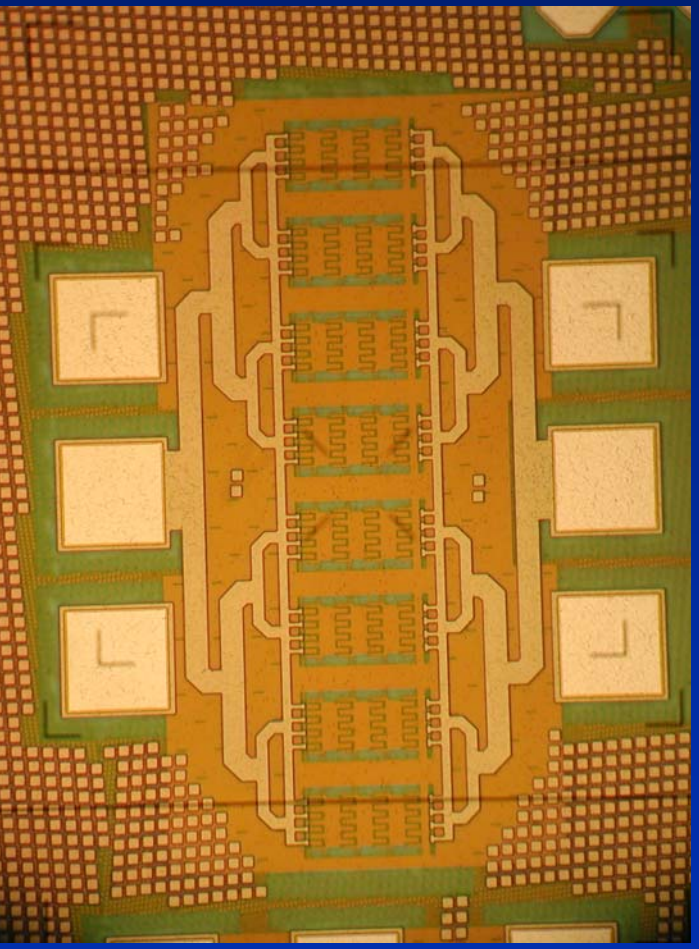
Power of 2 x 640µm HiFET at 1GHz

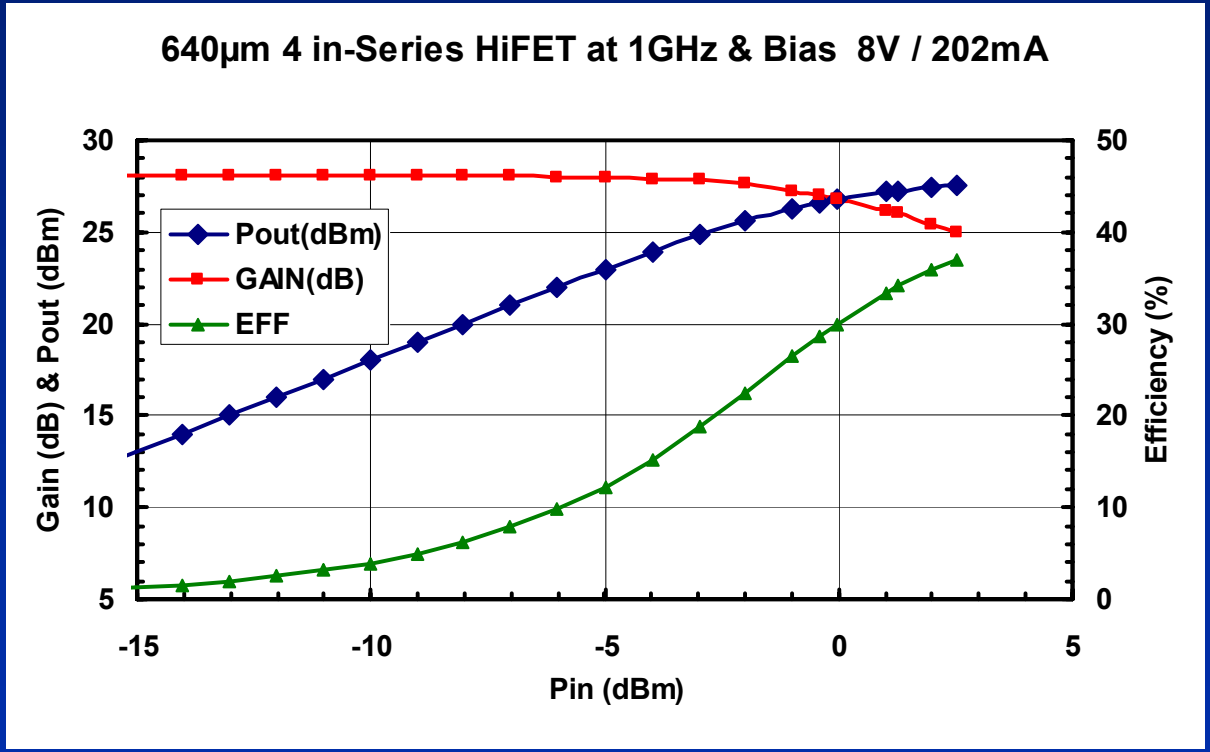




R_{opt}= 20 Ω

Power of 4 x 640µm HiFET at 1GHz





R_{opt}= 40 Ω
(2.5 Ω for 2560µm device)

Power and Gain Results at 1GHz

Parameter	80 µm CMOS	2 x 80 µm HiFET	4 x 80 µm HiFET	640 µm CMOS	2 x 640 µm HiFET	4 x 640 µm HiFET
Gain	18.1dB	21.6dB	24.3dB	21.9dB	25.5dB	28dB
P_{1dB}	10.9dBm	14.2dBm	17.9dBm	17.3dBm	22.2dBm	26.6dBm
Efficiency At P_{1dB}	26.1%	27.7%	31.6%	16%	25%	28.7%
P_{sat}	12.9dBm	15.5dBm	19.3dBm	21.1dBm	24.1dBm	27.5dBm
Efficiency At P_{sat}	42.3%	39.4%	42.7%	47.5%	41.8%	36.9%

Conclusion

- HiFET devices using 0.18μm CMOS process are demonstrated
- The HiFET configuration is applicable to CMOS to overcome low-voltage operation and low power density
- HIFET could help integrating PA on Silicon
- Broadband PA on Silicon is feasible

Acknowledgement

- Jack Singer
- Thomas Shutt
- Dr. Cynthia Hanson & Dr. Dan Radek at DARPA