CMOS PA For Wireless Applications[1]

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Abstract

The purpose of this work is to investigate the feasibility of using CMOS PA for wireless communications such as cell phone, WiFi and WiMAX. Our result indicates that we have successfully demonstrated this feasibility.

CMOS is a good candidate for the wireless communication because it is the natural choice for base band, IF and receiver. If it can also serve as PA, it is possible to achieve large-scale integration to reduce the cost, size and weight of the communication hardware. The major difficulty for CMOS PA is to achieve high power at high frequencies. This is because at high frequencies, CMOS has low DC bias voltage of only about 2 volts. This low DC bias voltage has 2 effects: 1) Relatively low RF output power because of low DC input power for any reasonable value of DC current. 2) The optimum RF impedance is proportional to Vdc/Idc. Low DC voltage leads to low RF impedance, which is very difficult to match to 50 ohms without substantial loss. Furthermore, silicon substrate is usually conductive, which results in substantial additional loss at RF frequencies.

To overcome the above problems, several papers have addressed these problems by introducing balanced designs [1], push-pull [2] or high-voltage [3], but each has certain limitations. In this paper, we propose an innovative technique to connect identical CMOS devices both DC and RF in series to address the low DC bias voltage and low impedance problems. In this case, both the DC bias voltage and RF impedance are multiples of the number of devices in series, leading to High-voltage, high Impedance FET configuration. (HIFET) In addition, the amplification gain is increased from that of a single device G dB to G + 10Log_{10}(N) dB, where N is the number of devices in series, allowing the use of longer gate length HIFET device to achieve the same gain. HIFET configuration is described in details in [3]. To address the Silicon substrate loss issue, we have developed CMOS small-signal, and large-signal equivalent circuits by modifying the CMOS foundry DC equivalent circuit, and we have employed the N-well configuration to RF isolate the device from the substrate.

We successfully demonstrated 2-HIFET and 4-HIFET CMOS devices (2 & 4 devices in series), using 0.18µm CMOS process. The device building block consists of 8 gate fingers, 0.18µm x 10µm each, for a total gate width of 80µm. Eight building blocks were connected in parallel for a total gate width of 640µm. Figure 1 shows the schematic diagram of 4 devices in series. The RF models were modified by the addition of shunt resistors and capacitors to account for the substrate effect. Figure 2 shows the device layout for a single 80µm cell HIFET.

Figures 3 and 4 show the performance of 4 x 80µm, and 4 x 640µm HIFET at 1GHz. Table 1 is the summary of the test results. Table 1 show that the DC bias voltage of the 2 in series and 4 in series HIFET which is 2 and 4 times that of the single device. The gains of the 2 in-series and 4 in-series devices are 3dB and 6dB higher than the single device, respectively. The output power of the 2 in-series and 4 in-series devices is twice and 4 times that of the single device, as predicted by the HIFET theory.

In summary, we increased the DC bias voltage from 2V to 8V for a HIFET which has 4 devices in series. We have achieved 28dB small signal, 27.5dBm output power with 36.9% efficiency at 1GHz from a 4 x 640µm 4-HIFET. We believe that this result is the best reported for a CMOS PA at 8V and 1 GHz. Most importantly, we have demonstrated the feasibility of CMOS as the power device for wireless communications using the HIFET concept, coupled with the developed RF equivalent circuits and N-well configuration. This work will serve as the baseline information for the development of an actual PA for various wireless communication applications.

REFERENCES

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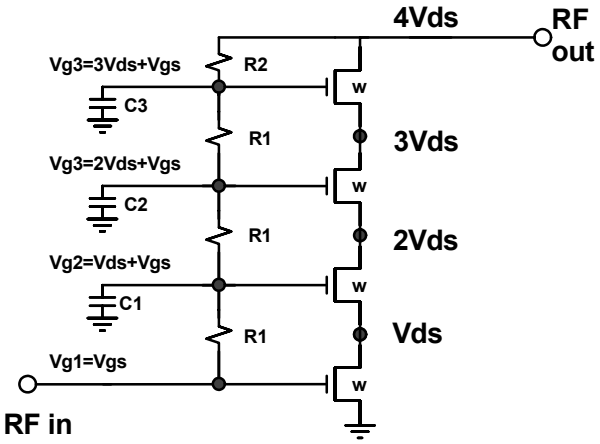

Figure 1: Four CMOS Connected Both RF and DC in Series

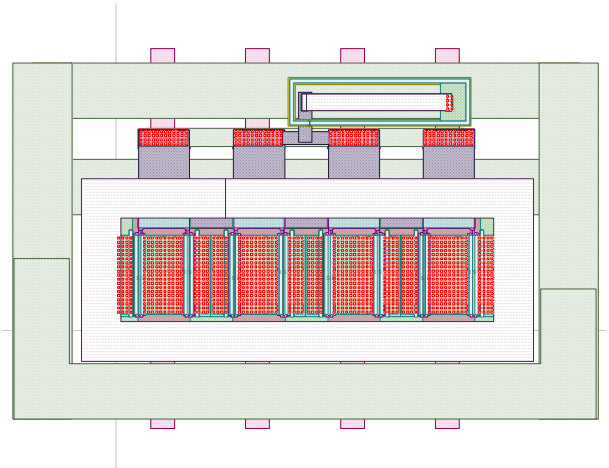

Figure 2: Eight Finger CMOS Device Layout

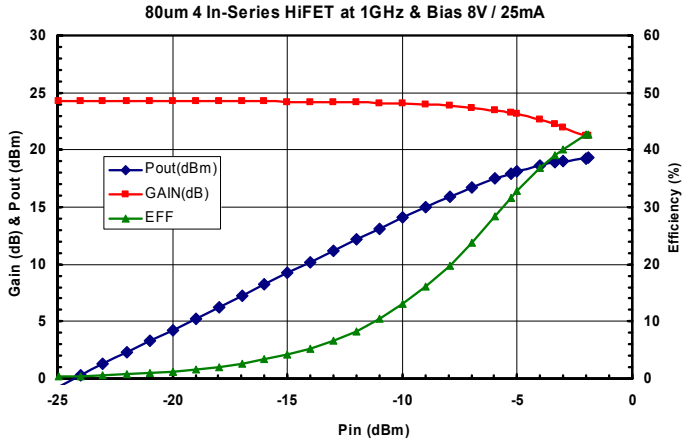

Figure 3: $P_{out,}$ & Eff. vs P_{in} of a 4 x 80µm HIFET at 1GHz

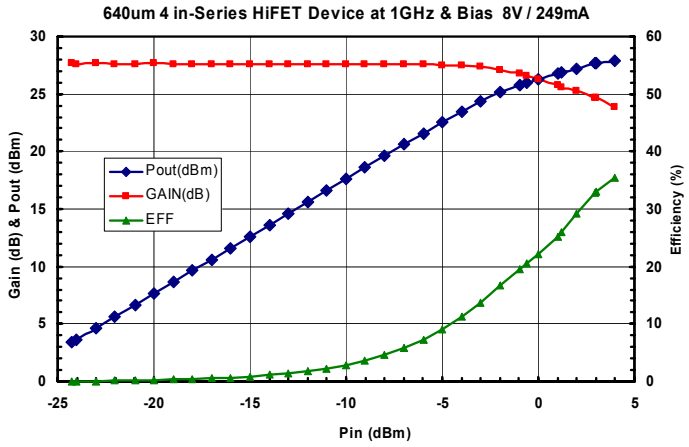

Figure 4: P_{out} & Eff. vs P_{in} of 4 x 640µm HiFET at 1GHz

Table 1: Summary of HIFET CMOS Performance

Parameter	**80 µm CMOS**	**2 x 80 µm HiFET**	**4 x 80 µm HiFET**	**640 µm CMOS**	**2 x 640 µm HiFET**	**4 x 640 µm HiFET**
DC bias voltage	2V	4V	8V	2V	4V	8V
Gain	18.1dB	21.6dB	24.3dB	21.9dB	25.5dB	28dB
P_{1dB}	10.9dBm	14.2dBm	17.9dBm	17.3dBm	22.2dBm	26.6dBm
Efficiency at P_{1dB}	26.1%	27.7%	31.6%	16%	25%	28.7%
P_{sat}	12.9dBm	15.5dBm	19.3dBm	21.1dBm	24.1dBm	27.5dBm
Efficiency at P_{sat}	42.3%	39.4%	42.7%	47.5%	41.8%	36.9%