

DESCRIPTION

AMCOM's AM183031WM-BM/FM-R is part of the GaAs MMIC power amplifier series. It has 30.5dB gain and 31.5dBm output power over the 1.6 to 3.3GHz band. This MMIC is in a ceramic package with both RF and DC leads at the lower level of the package to facilitate low-cost SMT assembly to the PC board. When mounting directly to PCB, please see application note AN700 for instructions. Because of high DC power dissipation, we recommend to mount these devices directly on a metal heat sink. The AM183031WM-EM is a drop-in package with straight leads. The AM183031WM-FM-R is the AM183031WM-BM-R mounted on a gold-plated copper flange carrier. There are two screw holes on the flange to facilitate screwing on to a metal heat sink. This MMIC is RoHS compliant.

FEATURES

- Wide bandwidth from 1.7 to 3.5GHz
- High output power, P1dB = 31.5dBm
- High gain, 30.5dB
- Fully matched; 50-ohm input/output impedance

APPLICATIONS

- Wireless Internet Access
- Wireless Local Loop
- MMDS

PERFORMANCE* ($V_{ds} = 8V$, $I_{dq} = 750mA$, $V_{gs} \approx -0.6V$, $T_a = 25^\circ C$)

Parameters	Minimum	Typical	Maximum
Frequency	1.8 – 3.0GHz	1.7 – 3.5GHz	
Gain (Small signal)	27dB	30.5dB	
Gain Ripple		$\pm 1.0dB$	$\pm 2.0dB$
P1dB	28.5dBm	30.5dBm	
P3dB	29Bm	31.5dBm	
IP3	-	40.0dBm	
Noise Figure	-	< 7.5dB	
Gain vs Temperature		-0.05 dB/ $^\circ C$	-
Efficiency @ P1dB	-	20%	
Input Return Loss	15dB	18dB	
Output Return Loss	10dB	12dB	
Thermal Resistance		11.7 $^\circ C/W$	

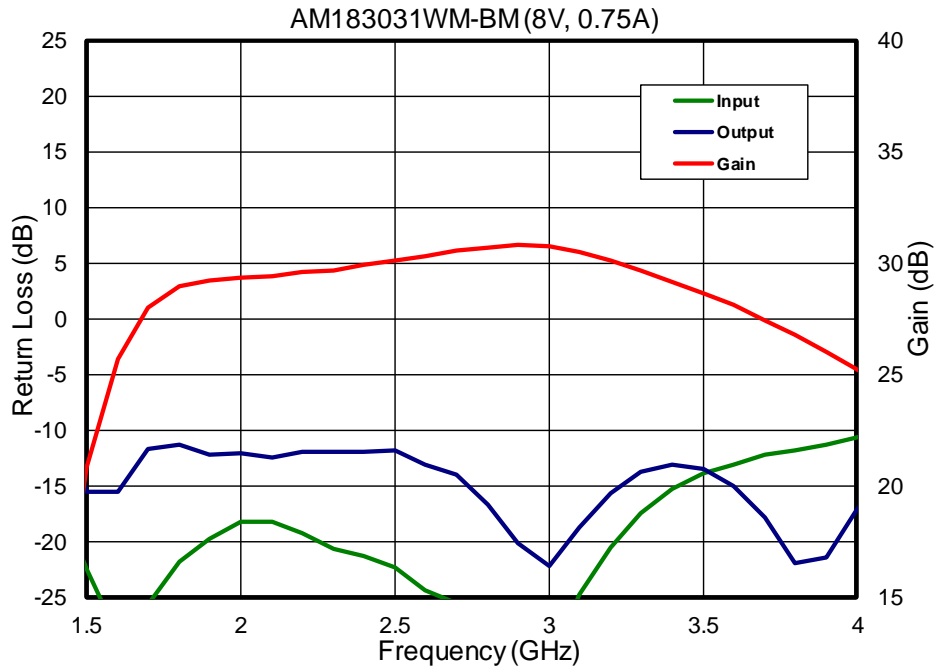
* Specifications subject to change without notice

ABSOLUTE MAXIMUM RATING

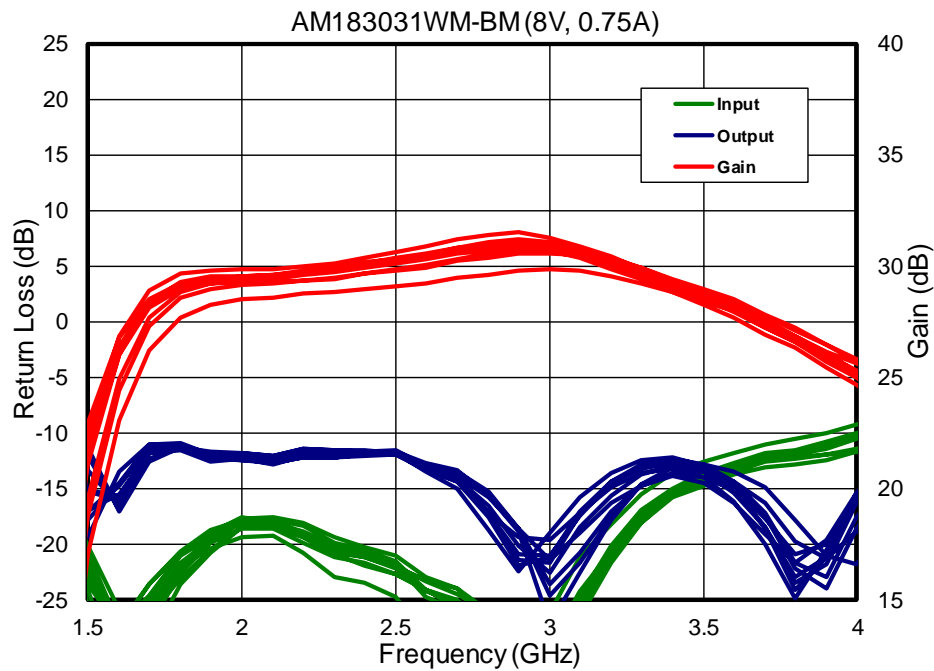
Parameter	Symbol	Rating
Drain source voltage	V_{ds}	10V
Gate source voltage	V_{gs}	-5V
Drain source current	I_{ds}	1.3A
Continuous dissipation at room temperature	P_t	12.8W
Channel temperature	T_{ch}	175°C
Storage temperature	T_{sto}	-55°C to +135°C

SMALL SIGNAL DATA*

a) Average



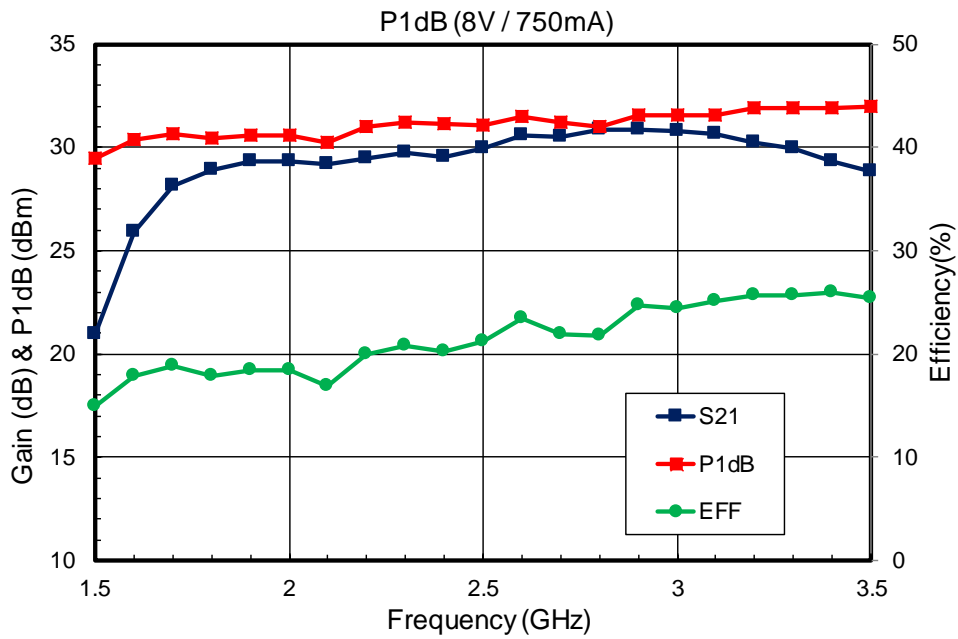
b) Variations



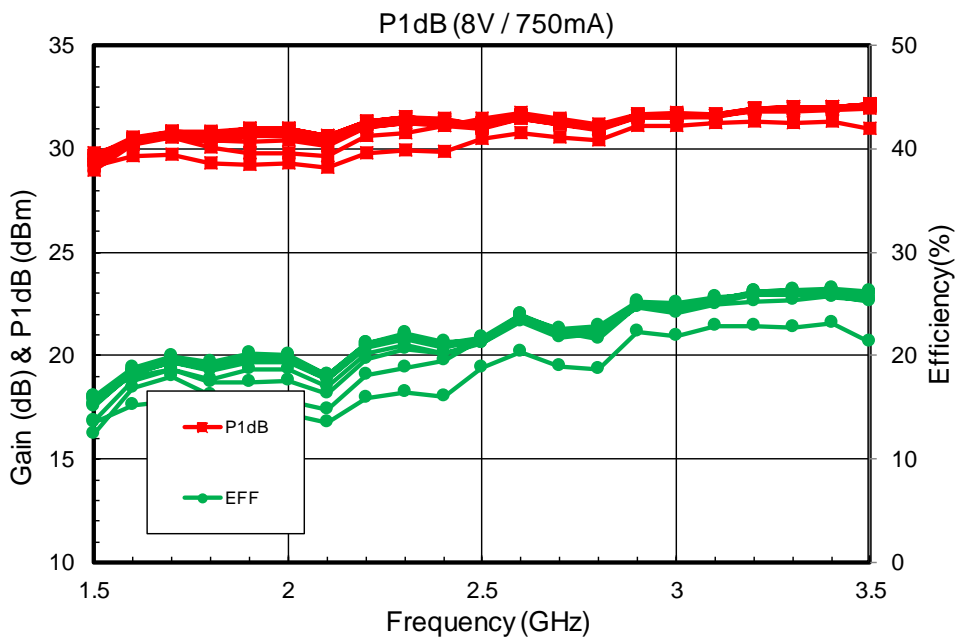
* Specifications subject to change without notice

POWER DATA*

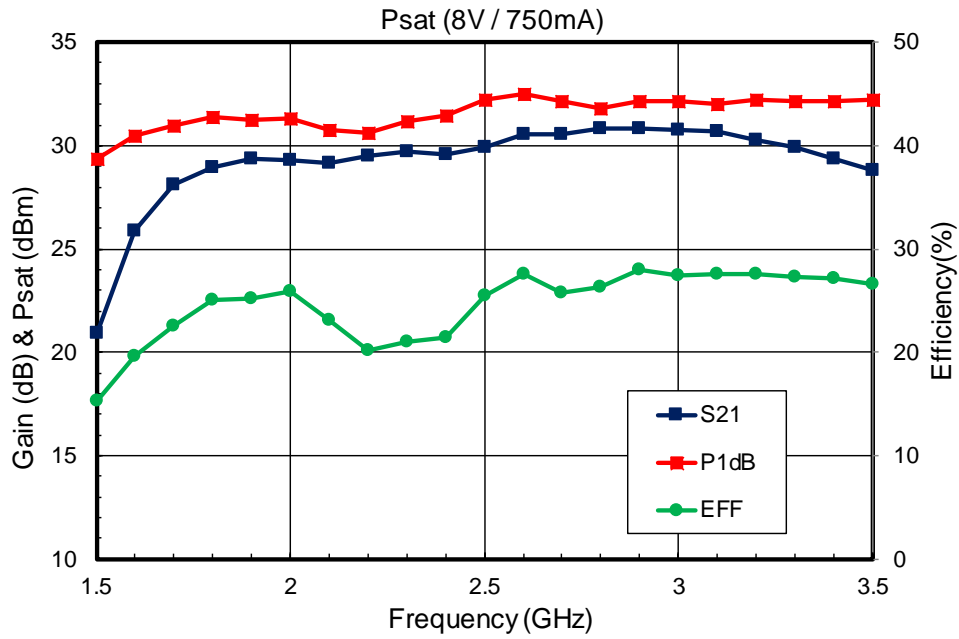
a) Average P1dB



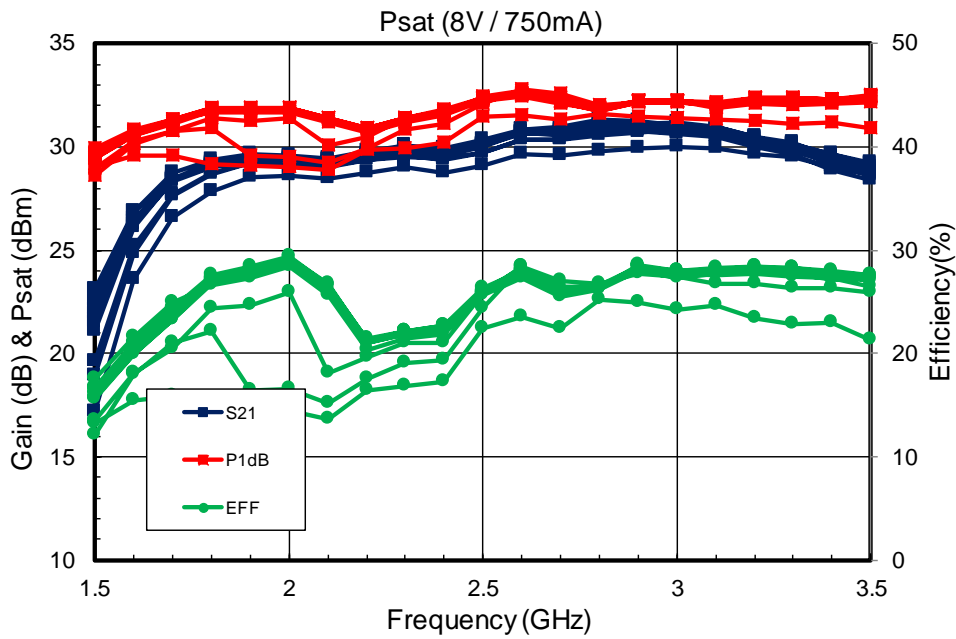
b) P1dB Variation



c) Average Psat

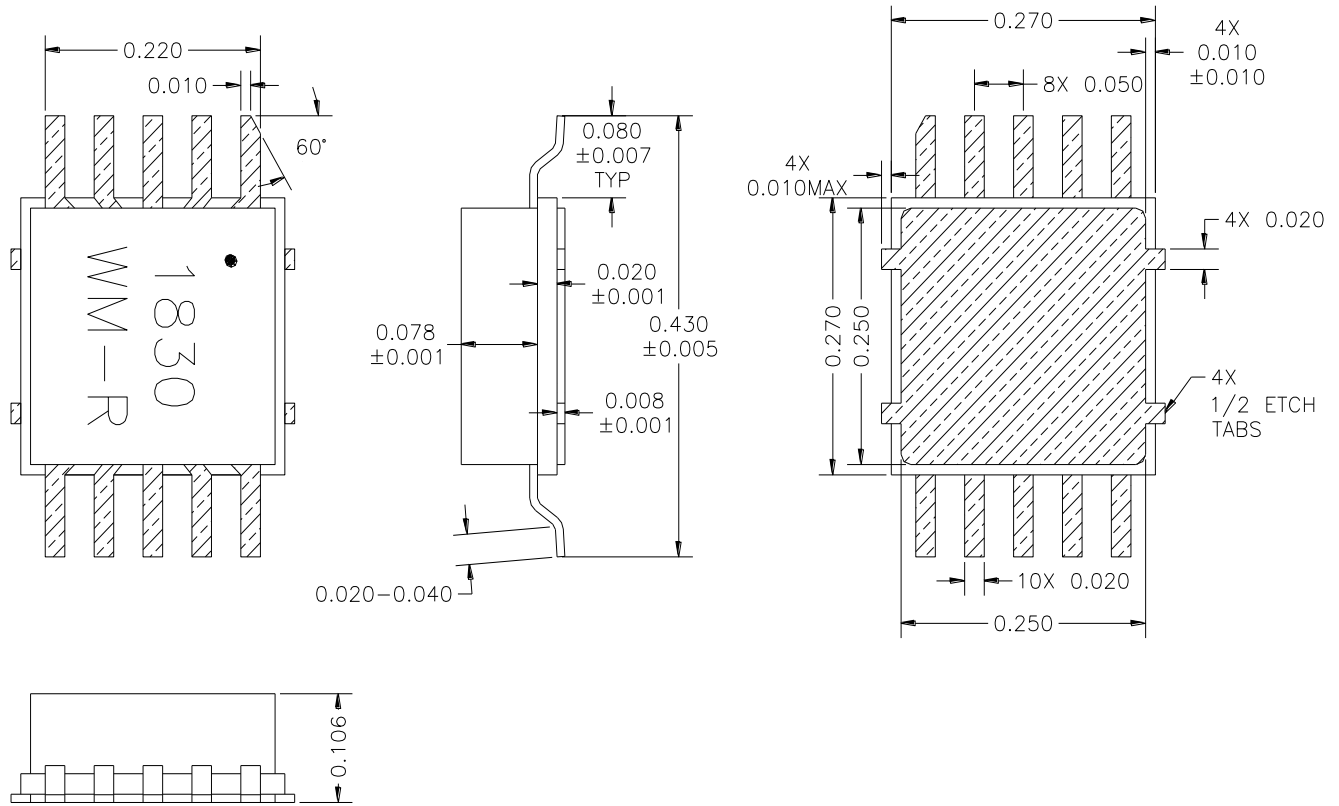


d) Psat Variation

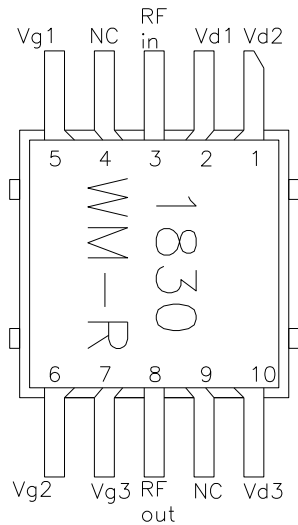


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BM PACKAGE OUTLINE



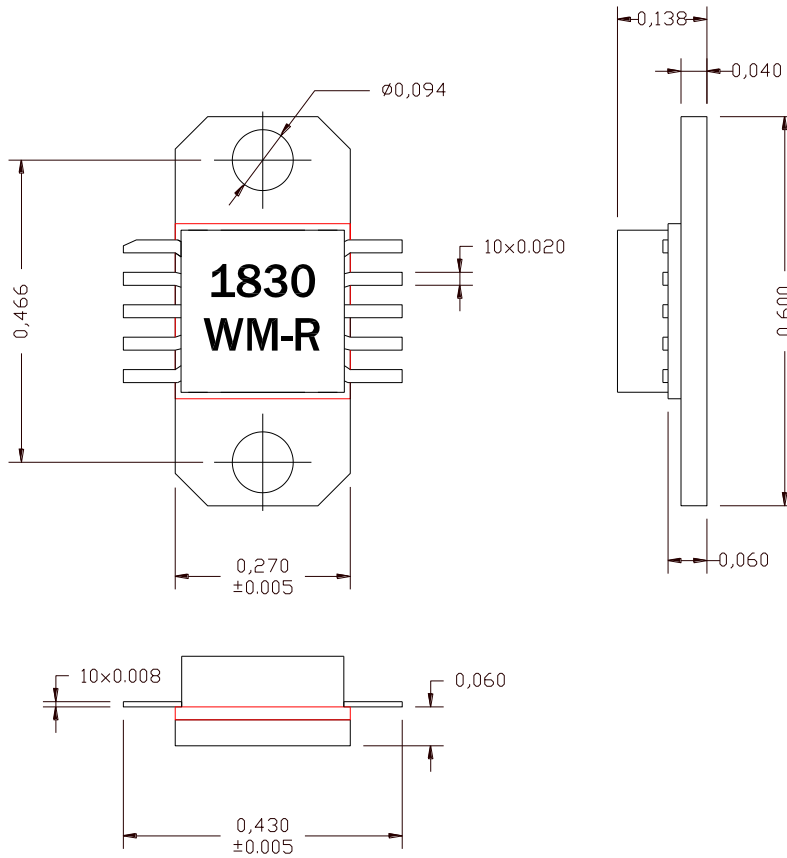
PIN LAYOUT



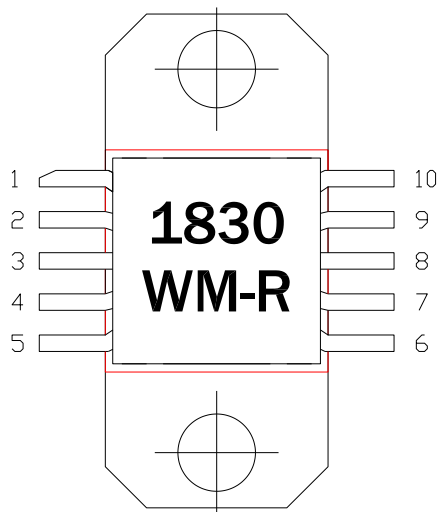
Pin No.	Function
1	Vds2
2	Vds1
3	RF in
4	NC
5	Vgs1
6	Vgs2
7	Vgs3
8	RF
9	NC
10	Vds3

* Gate voltage may vary from lot to lot

EM PACKAGE OUTLINE



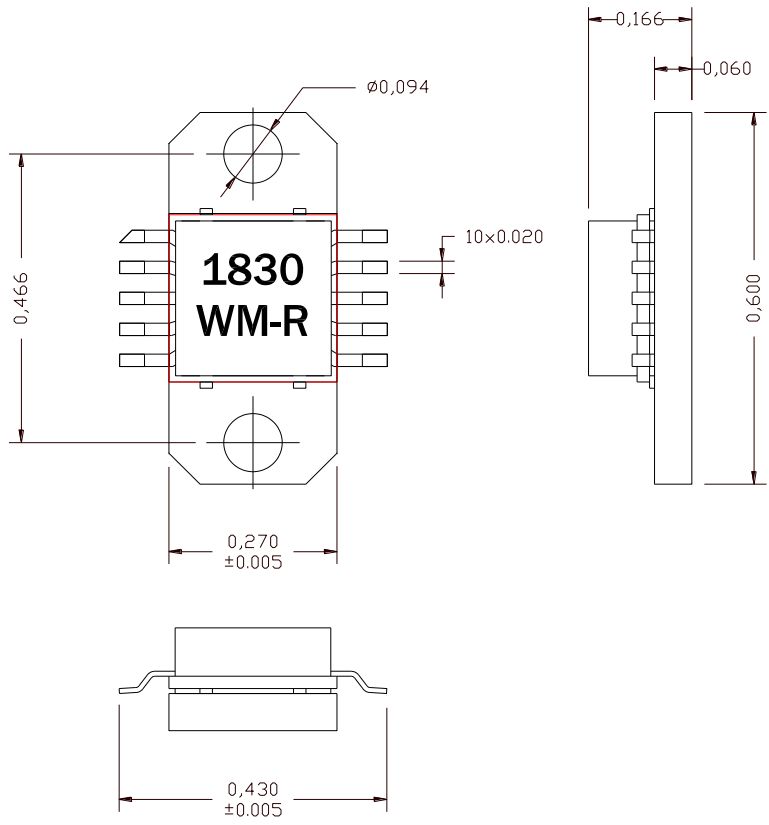
PIN LAYOUT



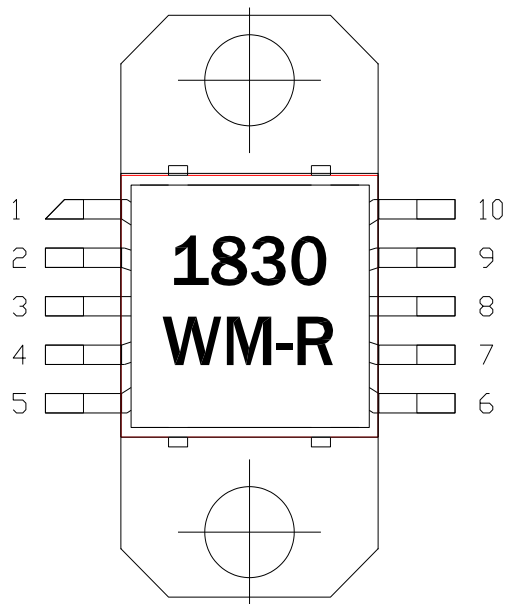
Pin No.	Function
1	Vds2
2	Vds1
3	RF in
4	NC
5	Vgs1
6	Vgs2
7	Vgs3
8	RF
9	NC
10	Vds3

* Gate voltage may vary from lot to lot

FM PACKAGE OUTLINE



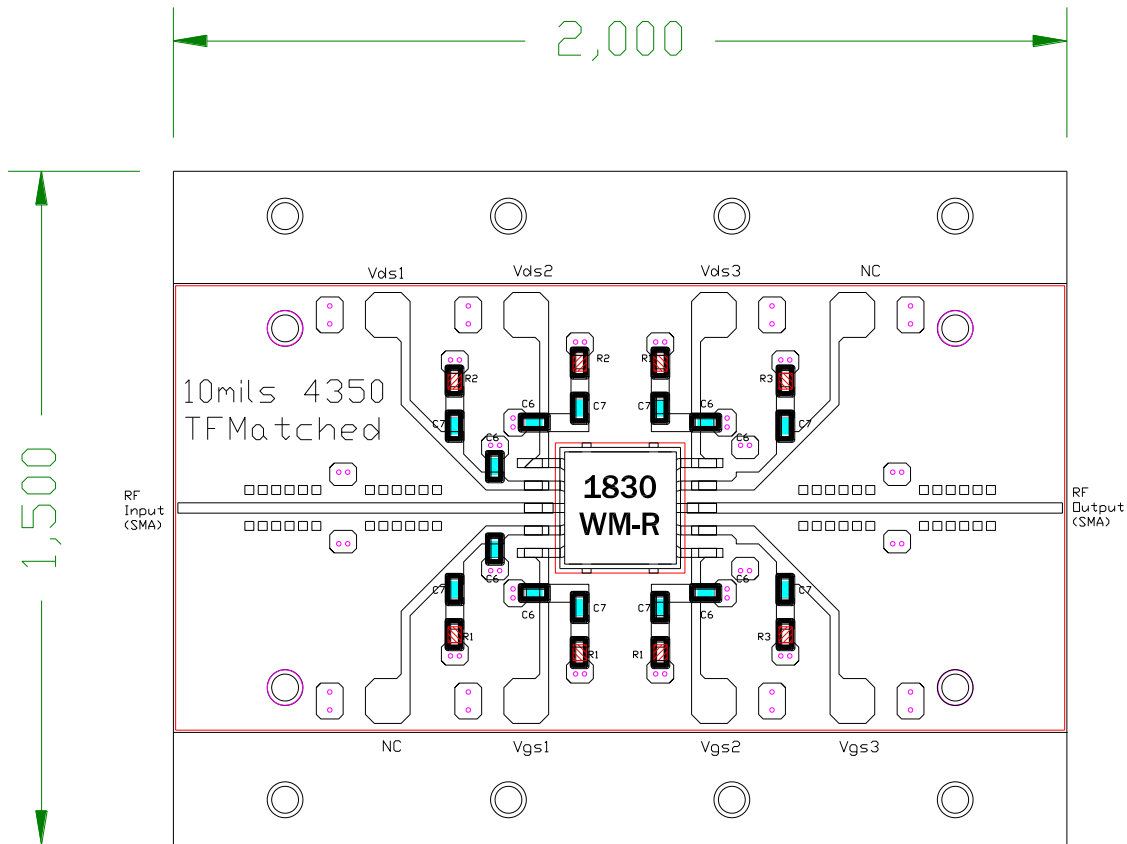
PIN LAYOUT



Pin No.	Function
1	Vds2
2	Vds1
3	RF in
4	NC
5	Vgs1
6	Vgs2
7	Vgs3
8	RF
9	NC
10	Vds3

* Gate voltage may vary from lot to lot

TEST CIRCUIT OUTLINE for BM Package

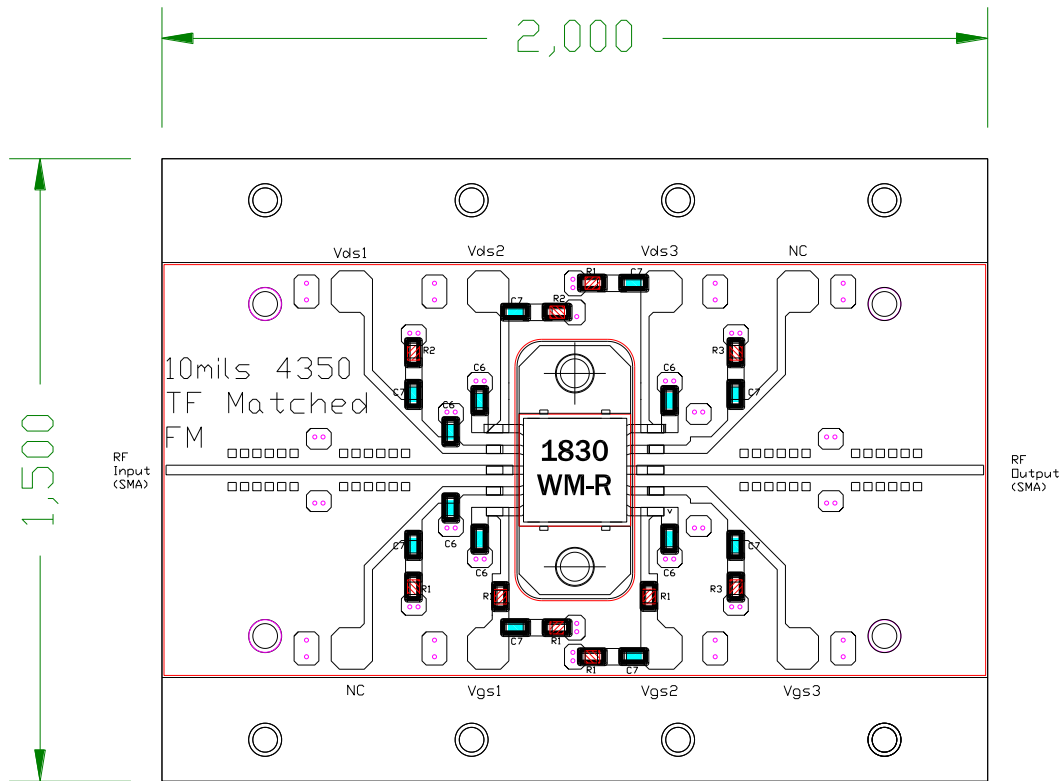


- Notes:
- 1- 10mils Rogers 4350 Material epoxied
 - 2- Ckt is for matched MMICs
 - 3- C6=20pF, C7=1000pF,
R1=50ohms, R2=10ohms, R3=5ohms
 - 4- All Caps & Resistors are 0603 size

Important Notes:

- 1- The MMIC should have a good heat sink to avoid overheating. If SMT is used use PC board thickness ≤ 10 mils and ensure vias are filled with solder or metal to lower PCB heat resistance. MMIC could be attached on direct ground for lowest junction temperature.
- 2- Recommended current biases are 70mA, 150mA & 450mA for the first, second and third stages respectively.
- 3- Do not apply V_{ds1} , V_{ds2} & V_{ds3} without proper negative voltages on V_{gs1} , V_{gs2} & V_{gs3} .
- 4- The currents flowing out of the V_{gs1} , V_{gs2} & V_{gs3} pins are less than 70 μ A, 150 μ A & 3mA at P_{1dB} .
- 5- External 1 μ F dipped tantalum capacitor should be attached to $V_{ds1,2,3}$ and $V_{gs1,2,3}$ to decouple external bias leads.

TEST CIRCUIT for EM & FM package



- Notes:
- 1- 10mils Rogers 4350 Material epoxied
 - 2- Ckt is for matched MMICs
 - 3- C6=20pF, C7=1000pF,
R1=50ohms, R2=10ohms, R3=5ohms
 - 4- All Caps & Resistors are 0603 size

Important Notes:

- 1- The MMIC flange should have a good heat sink to avoid overheating.
- 2- Recommended current biases are 80mA, 165mA & 500mA for the first, second and third stages respectively.
- 3- Do not apply V_{ds1} , V_{ds2} & V_{ds3} without proper negative voltages on V_{gs1} , V_{gs2} & V_{gs3} .
- 4- The currents flowing out of the V_{gs1} , V_{gs2} & V_{gs3} pins are less than 70 μ A, 150 μ A & 3mA at P_{1dB} .
- 5- External 1 μ F dipped tantalum capacitor should be attached to V_{ds} and V_{gs} to decouple external bias leads.