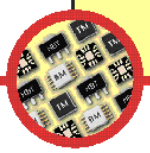
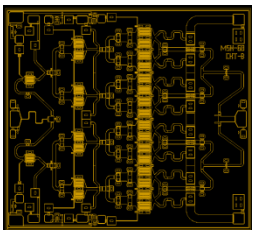
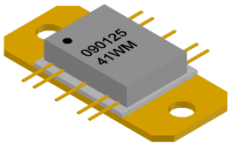
AM09012541WM-00
AM09012541WM-SN-R
January 2016
Rev 0

GaAs MMIC Power Amplifier



DESCRIPTION





AMCOM's AM09012541WM is a broadband GaAs MMIC power amplifier. It has 28dB small signal gain, and 41dBm output power over the 8 to 11GHz band at 8V bias and a 5% pulse operation. Because of high DC power dissipation, we strongly recommend to mount the bare die chip devices with eutectic bonding directly on a copper heat sink. It is capable of working at 8V DC bias voltage under pulsed condition if the eutectic bonding does not have any voids. Otherwise, we recommend operating the MMIC at 7V DC bias to provide some thermal margin. MMIC can be operated CW if drain voltage is dropped to +7V. The MMIC is offered in both chip (-00-R) and package (-SN-R) forms. The AM09012541WM-SN-R is in a ceramic package with a flange and straight RF and DC leads for drop-in applications. Good heat sinking is required. Both chip and packaged versions are RoHS compliant. The gate bias is supplied from a single bias pad for simple biasing.

FEATURES

- Wide bandwidth from 9 to 12.5GHz
- 41dBm of saturated output pulsed power
- High gain, 28dB
- Input /Output matched to 50 Ohms

APPLICATIONS

- Commercial telecom transmission equipment
- Fixed microwave backhaul
- Commercial 2-way radio

TYPICAL PERFORMANCE * (V_{ds} = +8V (1mS, 5% duty), I_{dsq} = 3400mA, V_{gs} = -1V**)

Parameters	Minimum	Typical **	Maximum
Frequency		9 – 12.5GHz	
Small Signal Gain	25dB	28dB	33dB
Gain Ripple			± 3.0dB
P_{1dB} ***	38dBm	40dBm	
P_{3dB} ***	39dBm	41dBm	
Efficiency @ P_{3dB}		30%	
Noise Figure		-	10dB
IP3 @ 10GHz		48dBm	
Input Return Loss		15dB	
Output Return Loss		7dB	
Thermal Resistance		1.25 °C/W	

* Specifications subject to change without notice.
** Current may change from lot to lot. Adjust V_{gs} to get I_{dsq}= 3.4A.
*** Power data are pulsed results for 5% pulse duty cycle and 1mS pulse width.

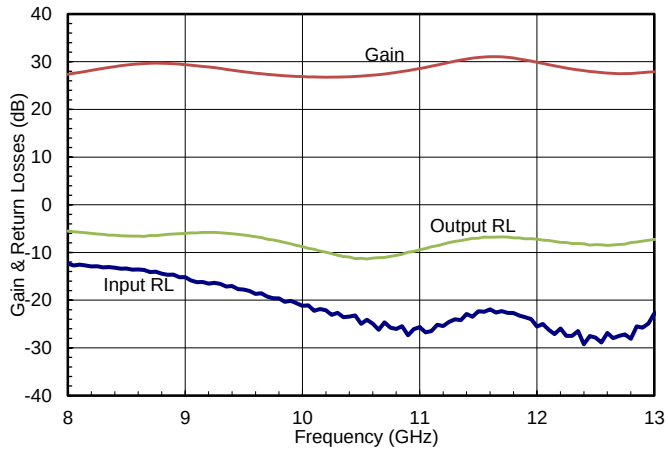
Email: info@amcomusa.com
Website: www.amcomusa.com
Tel. (301) 353-8400 Fax. (301) 353-8401
401 Professional Drive, Gaithersburg, MD 20879

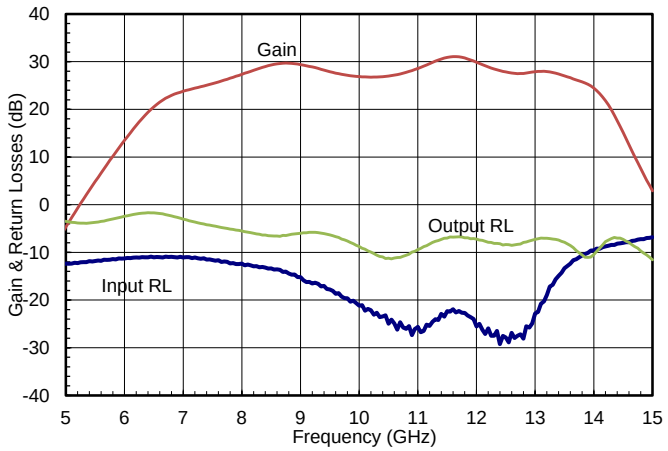
ABSOLUTE MAXIMUM RATING

Parameters	Symbol	Rating
Drain source voltage	$V_{ds1,2}$, V_{ds3}	9V
Gate source voltage	V_{gs}	-3V
Drain source current	$I_{dsq1,2}$	2A
Drain source current	I_{dsq3}	3.6A
Continuous dissipation at 25ºC	P_t	20W
Channel temperature	T_{ch}	175°C
Operating temperature	T_{op}	-55°C to +85°C
Storage temperature	T_{sto}	-55°C to +135°C

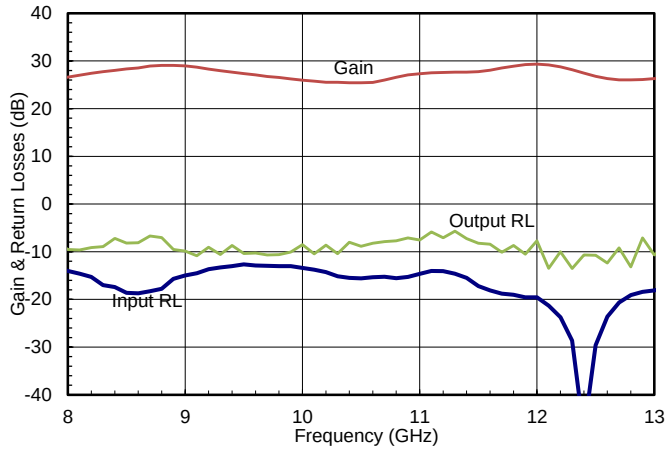
SMALL SIGNAL DATA*

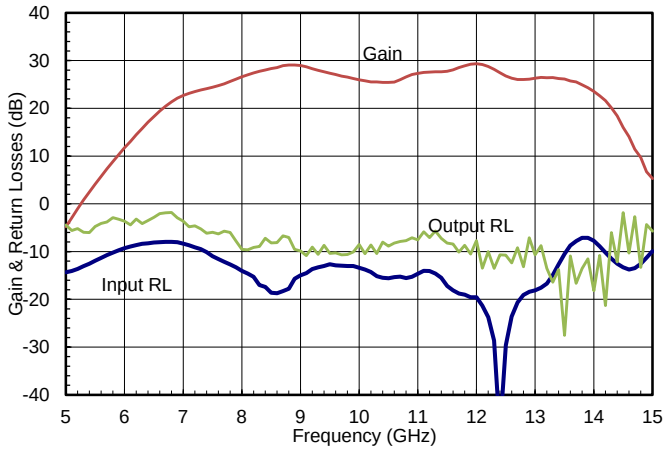
a) Chip S-Parameters (Bias: Vds= 5V, I_{dsq} = 2A, measured On-Wafer with RF probes)





b) Package S-Parameters (Bias: Vds= 5V, I_{dsq} = 2A)

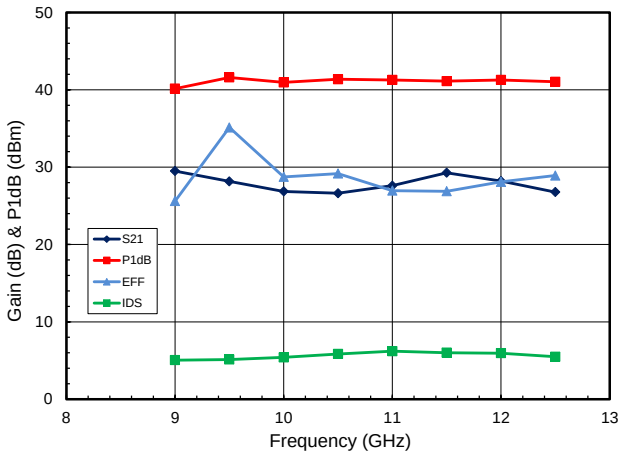


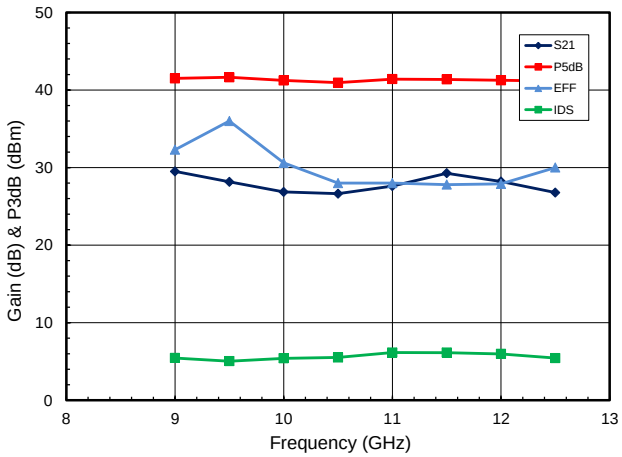


* MMIC could be operated from 5V to 8V without noticeable change in small signal performance.

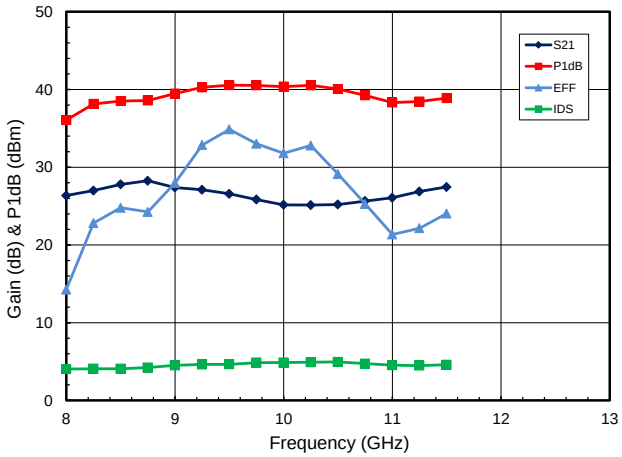
POWER DATA

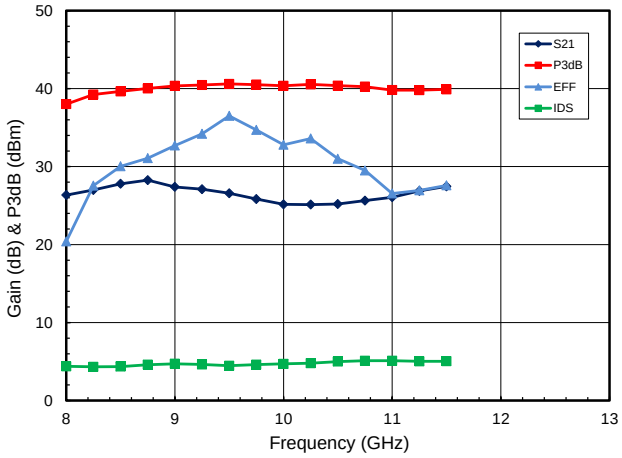
a) Chip Pulsed Power (V_{ds} = +8V , I_{dsq} = 3400mA, Pulse width is 1msec. , 5% duty)





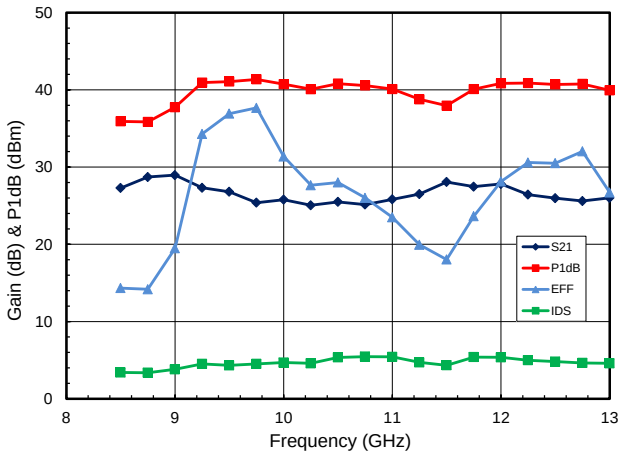
b) Chip CW Power (V_{ds} = +7V , I_{dsq} = 3400mA)

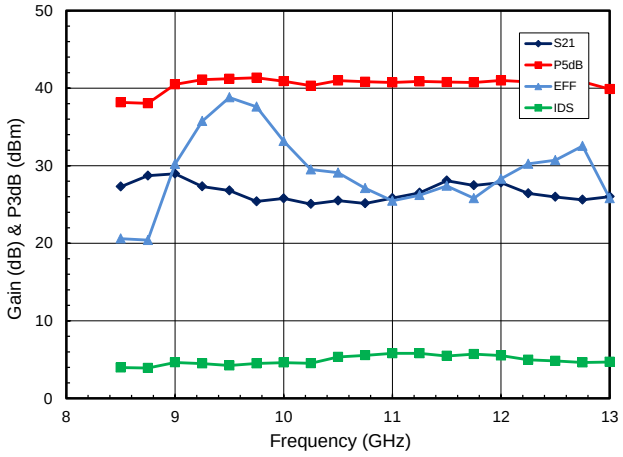




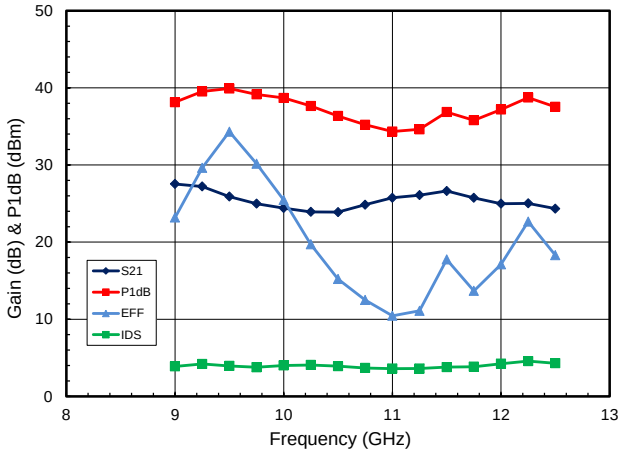
POWER DATA (cont.)

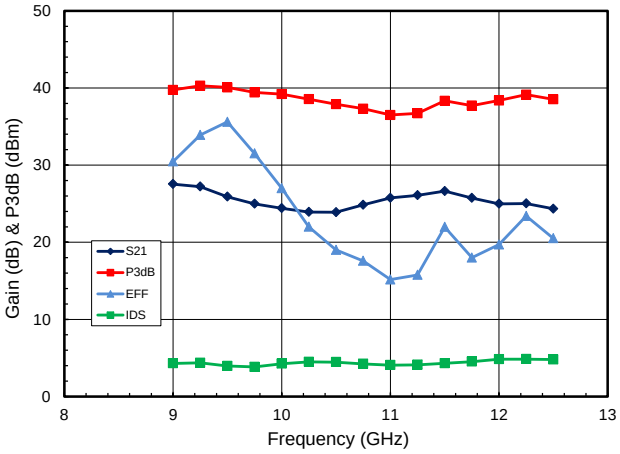
c) Package Pulsed Power (V_{ds} = +8V , I_{dsq} = 3400mA, Pulse width is 1msec. , 5% duty)





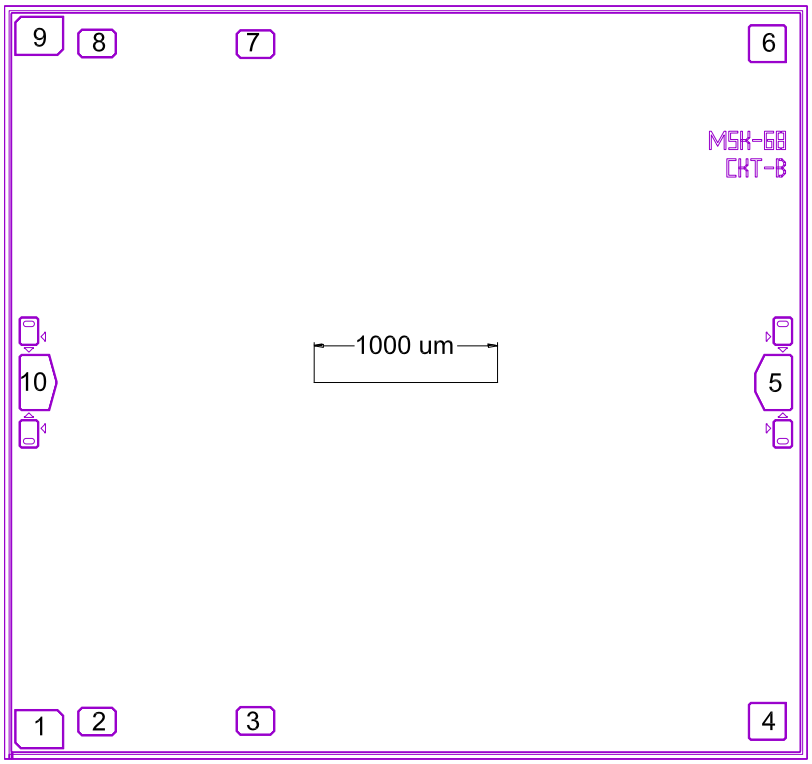
d) Package CW Chip Power (V_{ds} = +7V , I_{dsq} = 3400mA)





CHIP OUTLINE

CHIP DIM 4378x4108 um



Pin No.	Function	Bias
1	V_{gs}	-1V
2	V_{ds1}	+8V
3	V_{ds2}	+8V
4	V_{ds3}	+8V
5	RF out	NA
6	V_{ds3}	+8V
7	V_{ds2}	+8V
8	V_{ds1}	+8V
9	V_{gs}	-1V

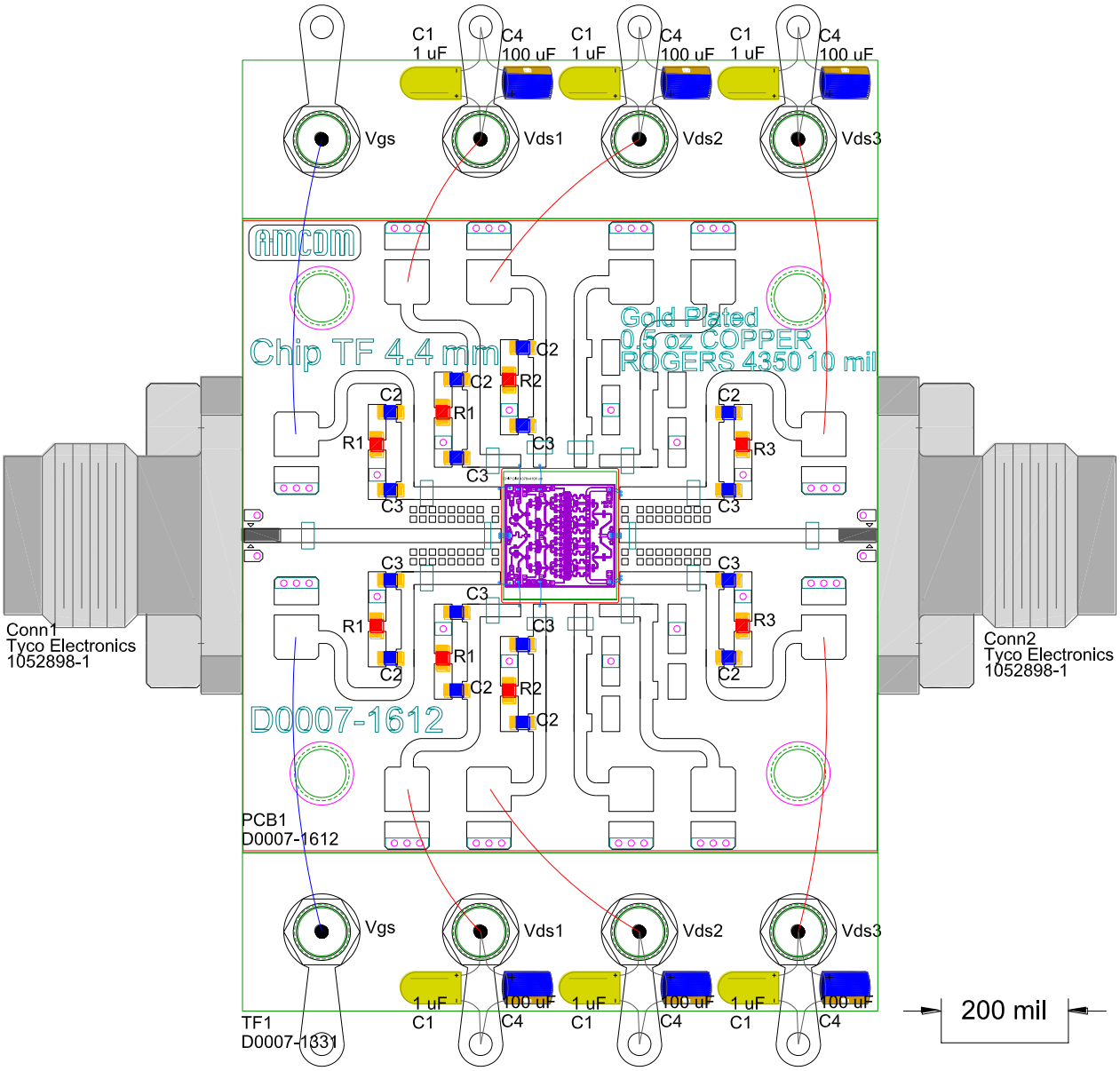
*Notes:

1- It is necessary to connect drain biases $V_{ds1,2,3}$ to both the upper and lower bonding pads.

2- V_{gs} bias value is for reference only and will vary slightly from one unit to another.

3- For CW operation use +7V for the drains.

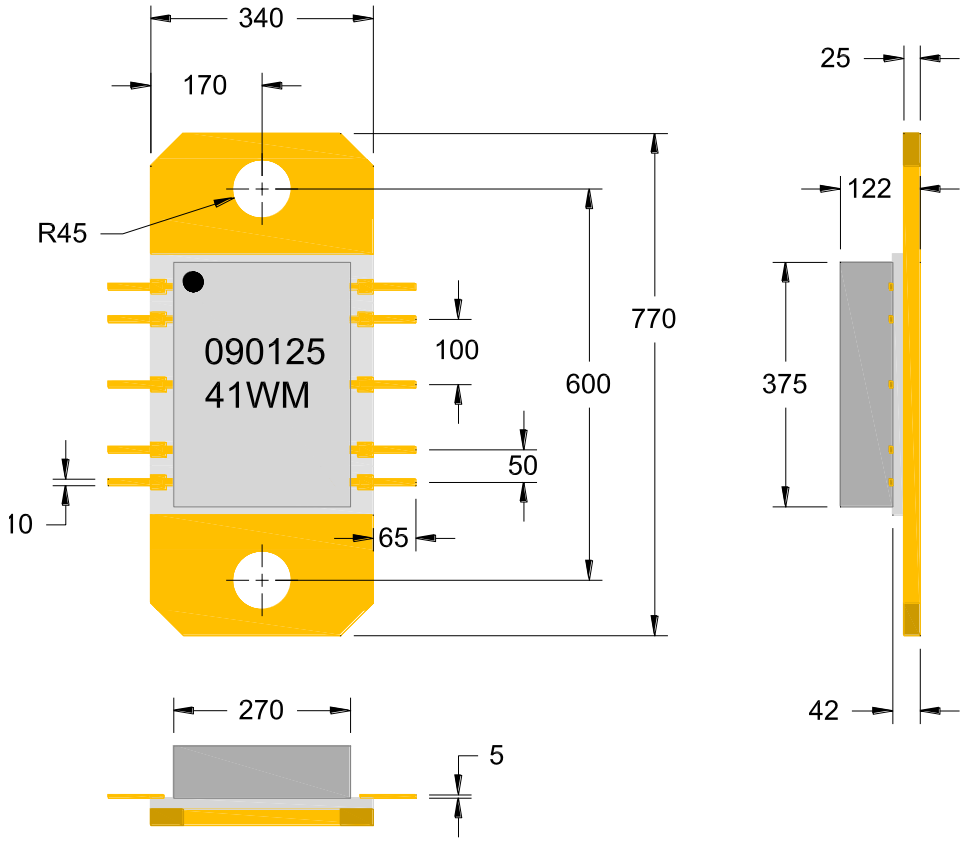
CHIP TEST FIXTURE



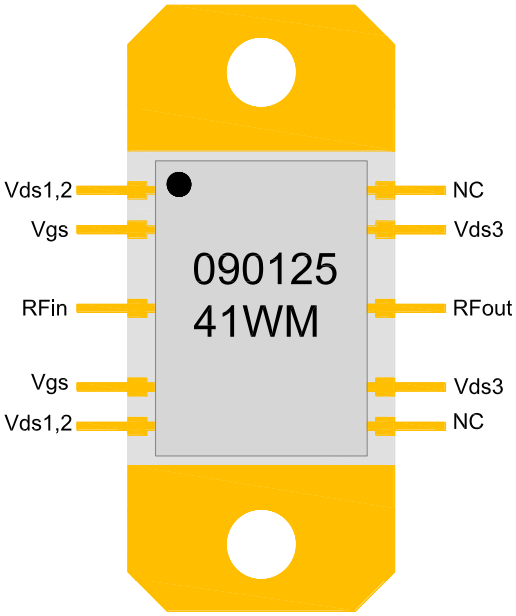
Notes:

1. Use epoxy to mount PCB, and eutectic soldering to mount chip.
2. C1=1µF (Dipped Radial Tantalum),C4=100uF(Aluminum Electrolytic) C2=1000pF, C3=20pF R1=50ohms, R2=10ohms, R3=5ohms.
3. This TF is designed for pulsing the gates, so if pulsing the drains instead, C1 and C4 have to be moved to the gate DC connectors.
4. All SMT Caps & Resistors are 0402 size.
5. Don't apply $V_{ds1,2,3}$ without proper negative voltages on V_{gs}.

SN PACKAGE OUTLINE (Dimensions in mils)

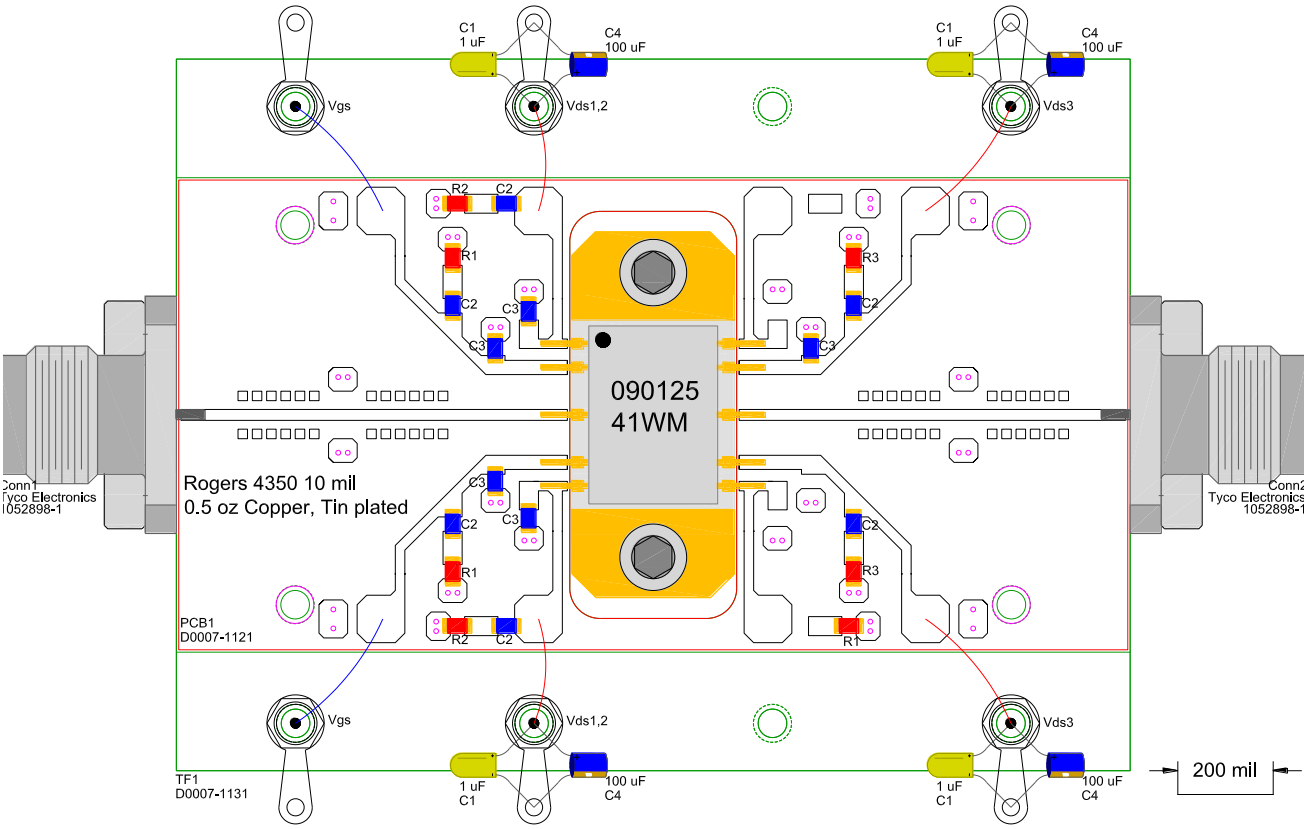


Pin Layout



Pin No.	Function	Bias
1	$V_{ds1,2}$	+8V
2	V_{gs}	-1V
3	RF out	NA
4	V_{gs}	-1V
5	$V_{ds1,2}$	+8V
6	NC	-
7	V_{ds3}	+8V
8	RF out	NA
9	V_{ds3}	+8V
10	NC	-

SN Package TEST FIXTURE



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3. This TF is designed for pulsing the gates, so if pulsing the drains instead, C1 and C4 have to be moved to the gate DC connectors.
4. All SMT Caps & Resistors are 0603 size.
5. Don't apply $V_{ds1,2,3}$ without proper negative voltages on V_{gs}.