

GaAs MMIC Power Amplifier AM08011041WM-00 AM08011041WM-SN-R

June 2012 Rev 1



## DESCRIPTION

AMCOM's AM08011041WM-00 (SN-R) is a broadband GaAs MMIC power amplifier. It has 28dB small signal gain, and >41dBm output power over the 8.5 to 10.5GHz band at 8V bias under pulsed conditions (5% duty cycle, 1msec pulse width). The AM08011041WM-00 is an un-packaged bare die. Because of high DC power dissipation, we strongly recommend to mount these devices with eutectic bonding directly on a copper heat sink. It is capable of working at 8V DC bias voltage under pulsed condition if the eutectic bonding does not have any voids. Otherwise, we recommend operating the MMIC at 7V DC bias to provide some thermal margin. The AM08011041WM-SN-R is in a ceramic package with a flange and straight RF and DC leads for drop-in applications. Good heat sinking is required. Both chip and packaged versions are RoHS compliant.

#### FEATURES

- Wide bandwidth from 8 to 11GHz
- 41dBm of saturated output pulsed power
- High gain, 28dB
- Input /Output matched to 50 Ohms

## **APPLICATIONS**

- Fixed microwave backhaul
- Radar
- Satellite communications
- 2-way radio

#### TYPICAL PERFORMANCE \* ( $V_{ds} = +8V$ (1mS, 5% duty), $I_{dsq} = 4500$ mA, $V_{gg} = -1.8V^{**}$ )

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Parameters	Minimum	Typical **	Maximum
Frequency	8.5 – 10.5GHz	8 – 11GHz	
Small Signal Gain		28dB	32dB
Gain Ripple		± 2dB	± 3.0dB
P <sub>1dB</sub> ***	38dBm	39dBm	
P <sub>sat</sub> ***	40dBm	41dBm	
Efficiency @ P <sub>1dB</sub>		25%	
Noise Figure		-	10dB
IP3 @ 1GHz		48dBm	
Input Return Loss		15dB	
Output Return Loss		7dB	
Thermal Resistance		2.3℃/W	

\* Specifications subject to change without notice.

<sup>\*\*</sup> Current may change from lot to lot. Adjust  $V_{gs}$  to reach  $I_{dsq1}$ =300mA,  $I_{dsq2}$ =1.2A,  $I_{dsq3}$ =3.0A.  $V_{ds}$  8V is at the MMIC drain terminal. Because  $I_{ds}$  is over 5 Amp, if your test system has a 0.1-ohm resistance between the DC power supply and the MMIC drain, it will have a drop of 0.5V, which reduces output power. In this case, we recommend raising the DC power supply voltage to 8.5V.

\*\* Power data are pulsed results for 5% pulse duty cycle and 1mS pulse width.

#### **ABSOLUTE MAXIMUM RATING**

Parameters	Symbol	Rating
Drain source voltage	$V_{ds1}$ , $V_{ds2}$ , $V_{ds3}$	9V
Gate source voltage	V <sub>gg</sub>	-3V
Drain source current	I <sub>dsq1</sub>	0.35A
Drain source current	I <sub>dsq2</sub>	1.5A
Drain source current	I <sub>dsq3</sub>	5.0A
Continuous dissipation at 25ºC	Pt	45W
Channel temperature	T <sub>ch</sub>	175°C
Operating temperature	T <sub>op</sub>	-55°C to +85°C
Storage temperature	T <sub>sto</sub>	-55°C to +135°C

#### SMALL SIGNAL DATA\*



\* MMIC could be operated at lower than  $V_{ds}$ =+8V with almost same small signal parameters.



# $\textbf{POWER DATA} \; (Vd \; = \! 8V, \; Vg \; = \; -1.8V, \; \textbf{I}_{dsq1} \! = \! 300 \text{mA}, \; \textbf{I}_{dsq2} \! = \! 1.2\text{A}, \; \textbf{I}_{dsq3} \! = \! 3.0\text{A}, \; 1\text{mS}, \; 5 \; \% \; \text{duty}) \; \textbf{*}$

\* MMIC could be operated from 5 to 8V. All power data is pulsed with 5% duty cycle and 100 cycles per second.

## **CHIP OUTLINE (00)**



• Gate biases are for reference only and may vary from lot to lot

**Pin Layout** 



\*\* It is important to connect  $V_{ds}$  to both the upper and lower bonding pads, such as #4 and #6 for  $V_{ds3}$ , #3 and #7 for  $V_{ds3}$ 

 $V_{ds2}$ 

## CHIP TEST FIXTURE



#### **Important Notes:**

- 1- Recommended current biases are 0.3A , 1.2A and 3.0A for the first stage , second and third stage respectively. Gate bias of -1.8V is for reference only.  $V_{gg}$  could be adjusted to vary the currents going thru the MMIC.
- 2- Do not apply  $V_{ds1}$  &,  $V_{ds2}$  &  $V_{ds3}$  without proper negative voltages.
- 3- The currents flowing out of the two V<sub>gg</sub> pins are around 300mA.

## SN PACKAGE OUTLINE









Pin No.	Function	Bias
1	Vds1	+8V
2	Vgg	-1.8V
3	RF in	NA
4	Vgg	-1.8V
5	Vds1	+8V
6	Vds2	+8V
7	Vds3	+8V
8	RF out	NA
9	Vds3	+8V
10	Vds2	+8V

# **TEST CIRCUIT for SN Package**



#### **Important Notes:**

- 4- Recommended current biases are 0.3A , 1.2A and 3.0A for the first stage , second and third stage respectively. Gate bias of -1.8V is for reference only. V<sub>gg</sub> could be adjusted to vary the currents going thru the MMIC.
- 5- Do not apply  $V_{ds1}$  &,  $V_{ds2}$  &  $V_{ds3}$  without proper negative voltages.
- 6- The currents flowing out of the two  $V_{gg}$  pins are around 300mA.