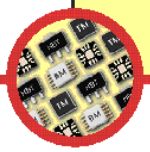
Gallium Nitride MMIC 20W 7.5 – 12.0 GHz Power Amplifier

AM07512043TM-00
AM07512041TM-SN
November 2015
Rev 1



DESCRIPTION

AMCOM's AM07512043TM-00 Chip is a broadband GaN MMIC power amplifier. It has 23dB gain, and 43 dBm output power over the 7.5 to 12.0GHz band. The AM07512041TM-SN-R is in a ceramic package with a flange and straight RF and DC leads for drop-in assembly. Because of high DC power dissipation, good heat sinking is required. The package is RoHS compliant. This MMIC is matched to 50 Ohms.

FEATURES

- Broadband from 7.5 to 12.0GHz
- Saturated output power Psat is 42dBm
- High gain, 23dB
- Input & output matched to 50 Ohms

APPLICATIONS

- Instrumentation
- Commercial telecom transmission equipment
- Fixed microwave backhaul

TYPICAL PERFORMANCE of BARE CHIP*

Parameters	Minimum	Typical **	Maximum
Frequency	8.0–11.5 GHz	7.5–12.0 GHz	
Small Signal Gain	19dB	23dB	
Gain Ripple		± 3.0dB	± 5.0dB
P1dB		38dBm	
Psat	40dBm	42.5dBm	
Psat Efficiency		30%	
Noise Figure		TBD	
IP3		TBD	
Input Return Loss		10dB	
Output Return Loss		10dB	
Thermal Resistance		1.0 °C/W	

* Specifications subject to change without notice.

** Bias Conditions is: V_{ds1} = +28V, I_{dsq1} = 0.36A, V_{ds2} = +28V, I_{dsq2} = 0.90A, V_{gs1} = V_{gs2} =-2.3V.

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TYPICAL PERFORMANCE OF PACKAGE at Vds=+28V*

Parameters	Minimum	Typical **	Maximum
Frequency	8.0–11.5 GHz	7.5–12.0 GHz	
Small Signal Gain	16dB	21dB	
Gain Ripple		± 3.0dB	± 5.0dB
P1dB		38dBm	
Psat	38dBm	41dBm	
Psat Efficiency		20%	
Noise Figure		TBD	
IP3		TBD	
Input Return Loss	9dB	>12dB	
Output Return Loss	5dB	>7dB	
Thermal Resistance		1.25 °C/W	

* Specifications subject to change without notice.

** Bias Conditions is: V_{ds1} = +28V, I_{dsq1} = 0.36A, V_{ds2} = +28V, I_{dsq2} = 0.90A, V_{gs1} = V_{gs2} =-2.3V.

TYPICAL PERFORMANCE OF PACKAGE at Vds=+15V*

Parameters	Minimum	Typical **	Maximum
Frequency	8.0–11.5 GHz	7.5–12.0 GHz	
Small Signal Gain	16dB	19dB	
Gain Ripple		± 3.0dB	± 5.0dB
P1dB		35dBm	
Psat	36dBm	38dBm	
Psat Efficiency		20%	
Noise Figure		TBD	
IP3		TBD	
Input Return Loss	9dB	>12dB	
Output Return Loss	5dB	>7dB	
Thermal Resistance		1.25 °C/W	

* Specifications subject to change without notice.

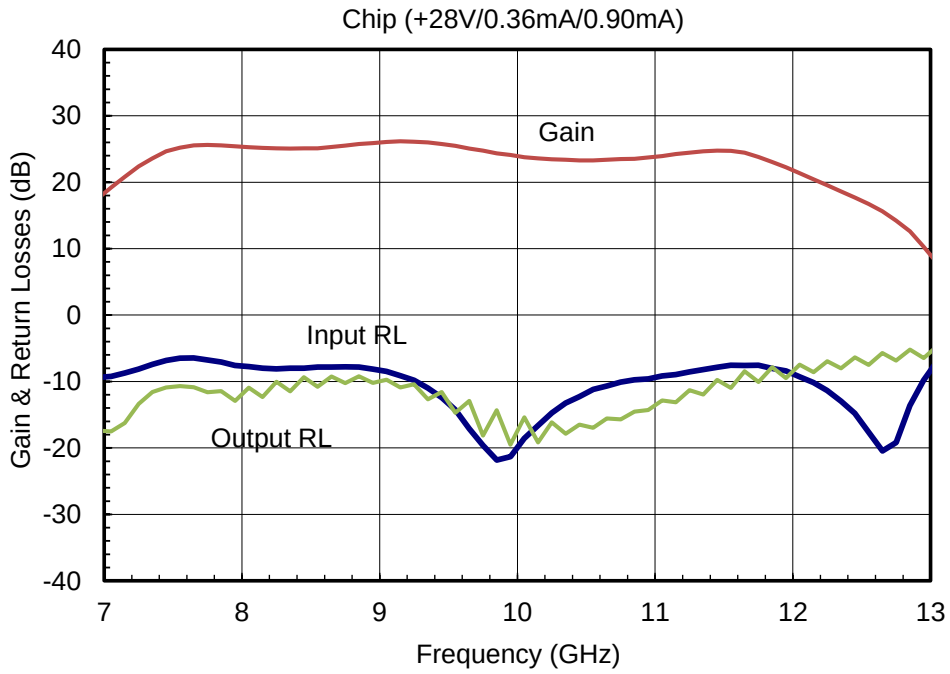
** Bias Conditions is: V_{ds1} = +15V, I_{dsq1} = 0.36A, V_{ds2} = +15V, I_{dsq2} = 0.90A, V_{gs1} = V_{gs2} =-2.3V

ABSOLUTE MAXIMUM RATING

Parameters	Symbol	Rating
First & second stage drain voltages	V_{ds1} , V_{ds2}	40V
Second stage drain voltage	V_{ds3}	40V
Gate source voltage	V_{gs1}& V_{gs2}	-6V
Drain source current	I_{dsq1} + I_{dsq2}	0.9A
Drain source current	I_{dsq3}	1.5A
Continuous dissipation at 25ºC	P_t	100W
Channel temperature	T_{ch}	200°C
Operating temperature	T_{op}	-55°C to +85°C
Storage temperature	T_{sto}	-55°C to +135°C

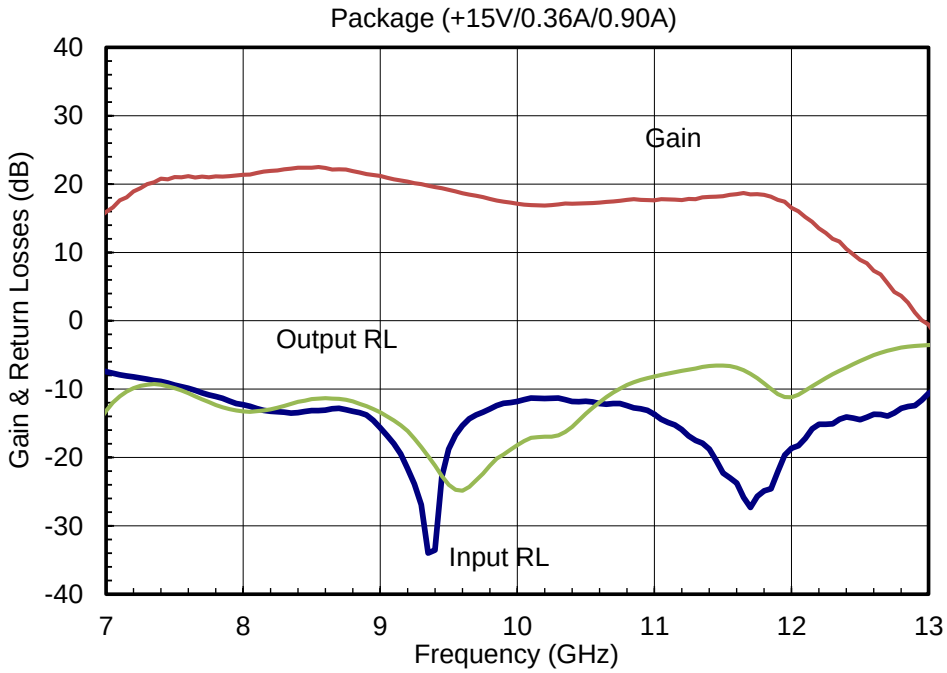
SMALL SIGNAL DATA

A) CHIP DATA*



* S-Parameters measured using test fixture. Bias is V_{ds1} = V_{ds2} = +28V , I_{ds1} =360mA , I_{ds3}=900mA , V_{gs1} = V_{gs2} =-2.3V .

B) PACKAGE DATA*



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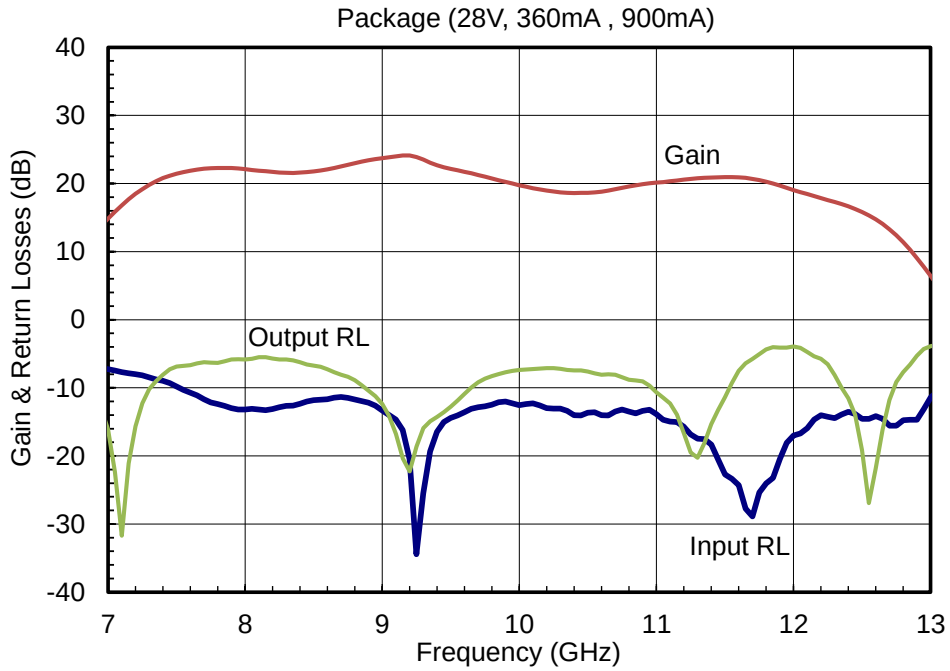

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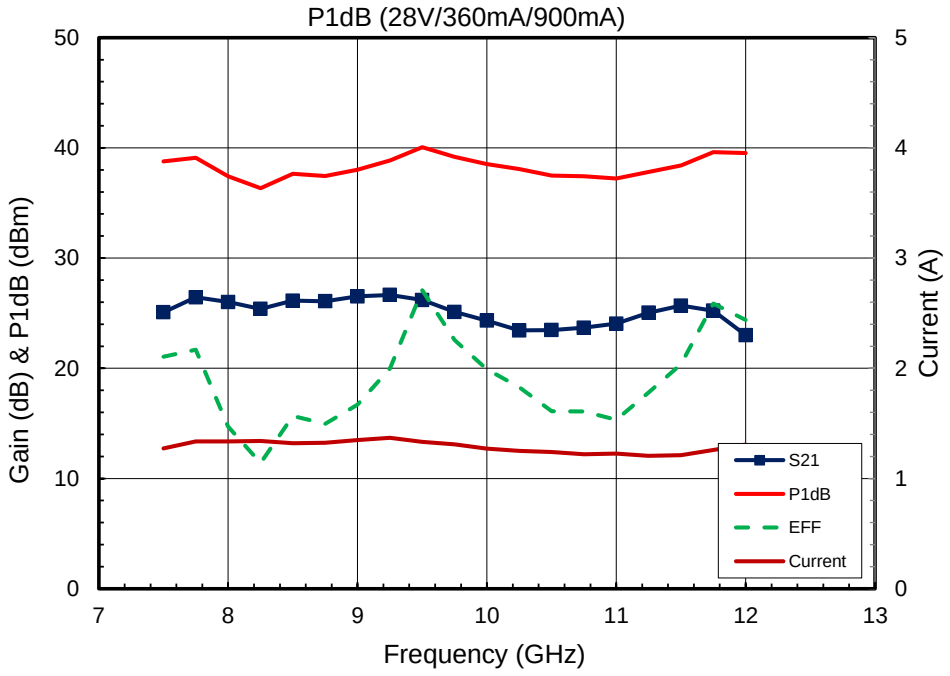
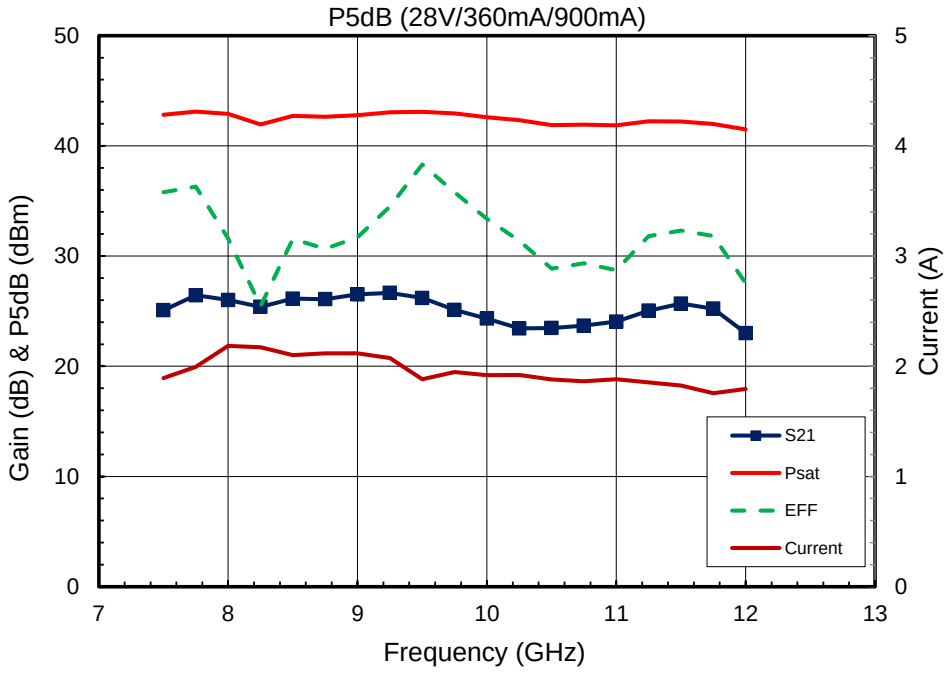
NOISE DATA
(TBD)

POWER DATA

A) CHIP DATA





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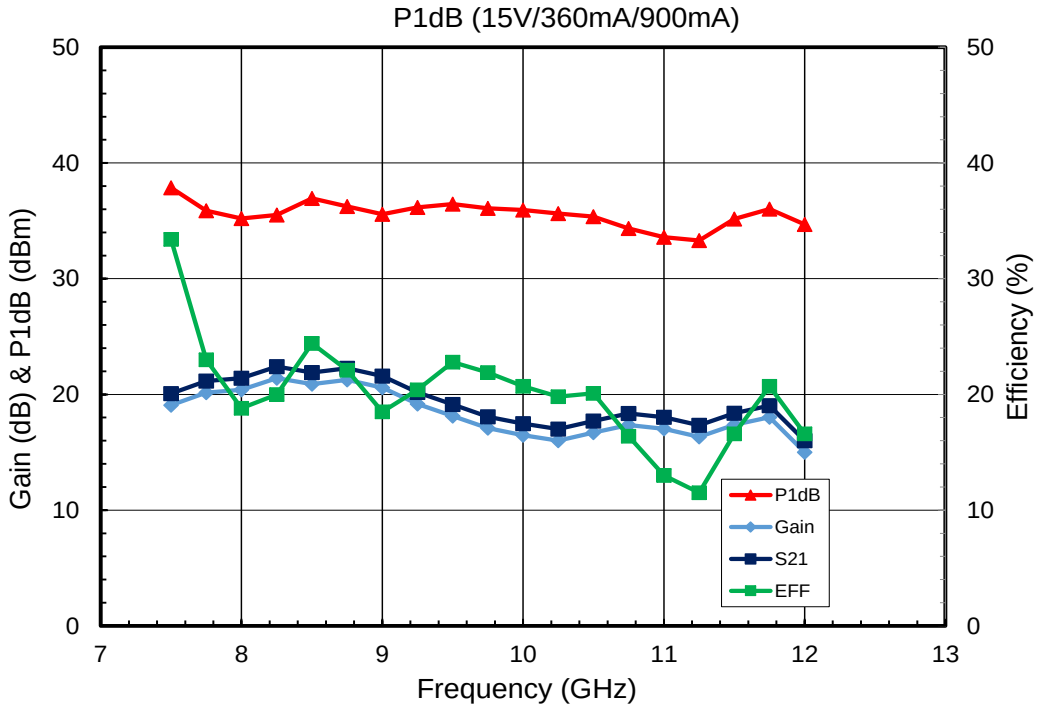
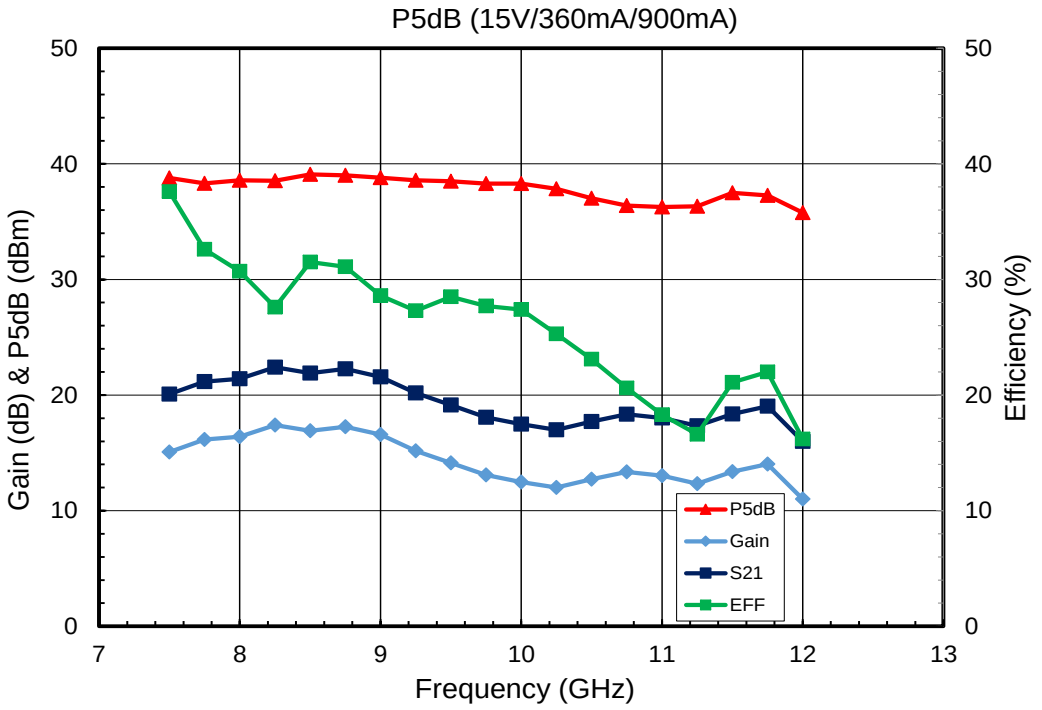
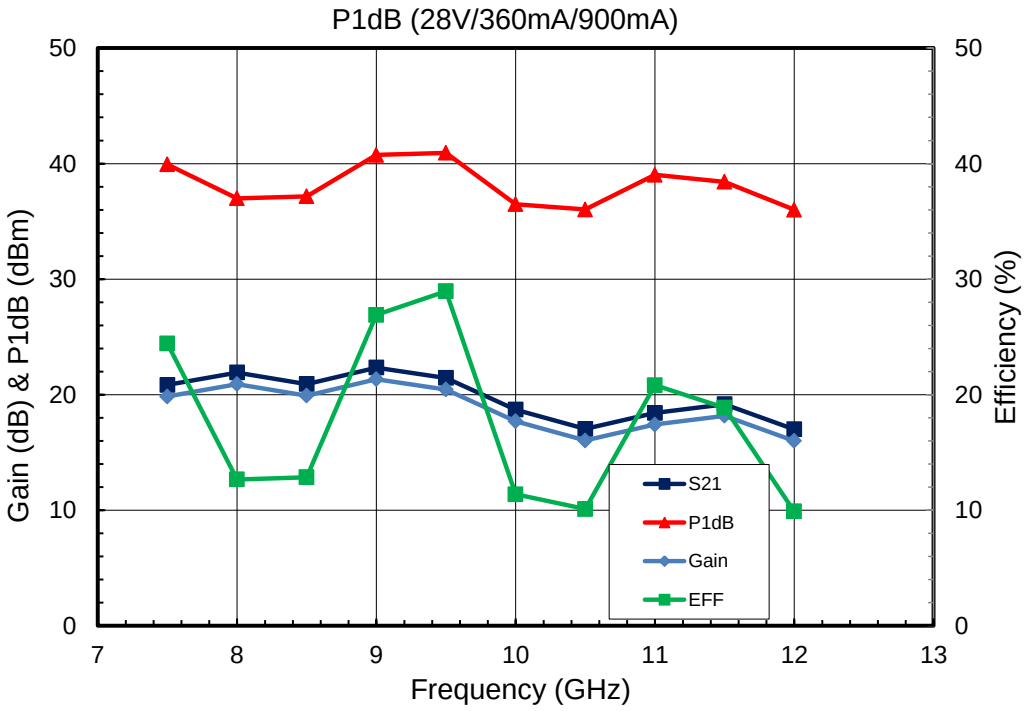
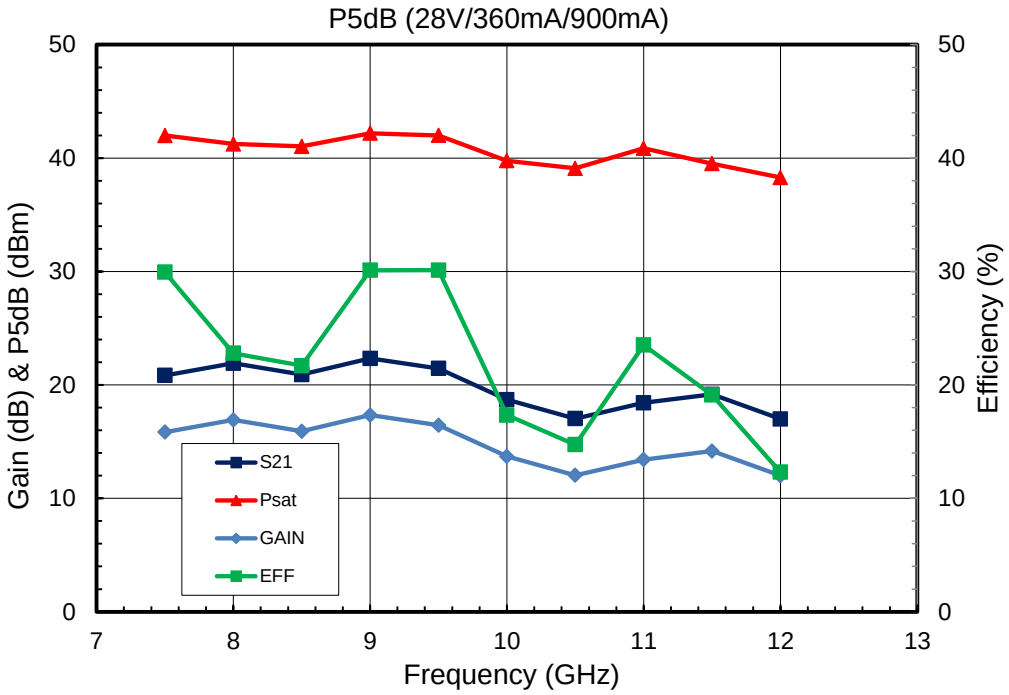
B) PACKAGE DATA



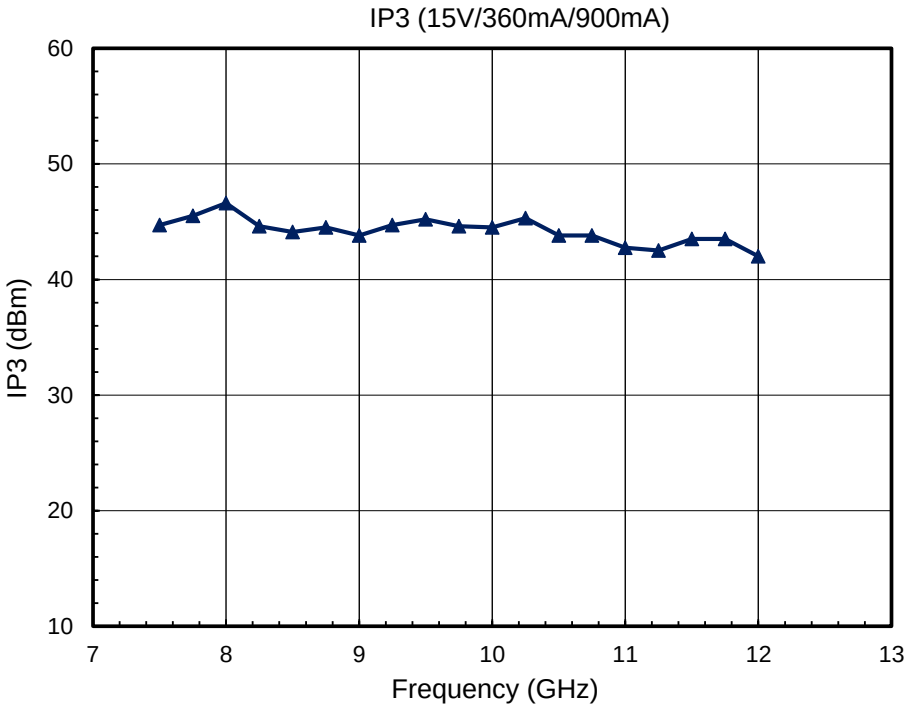


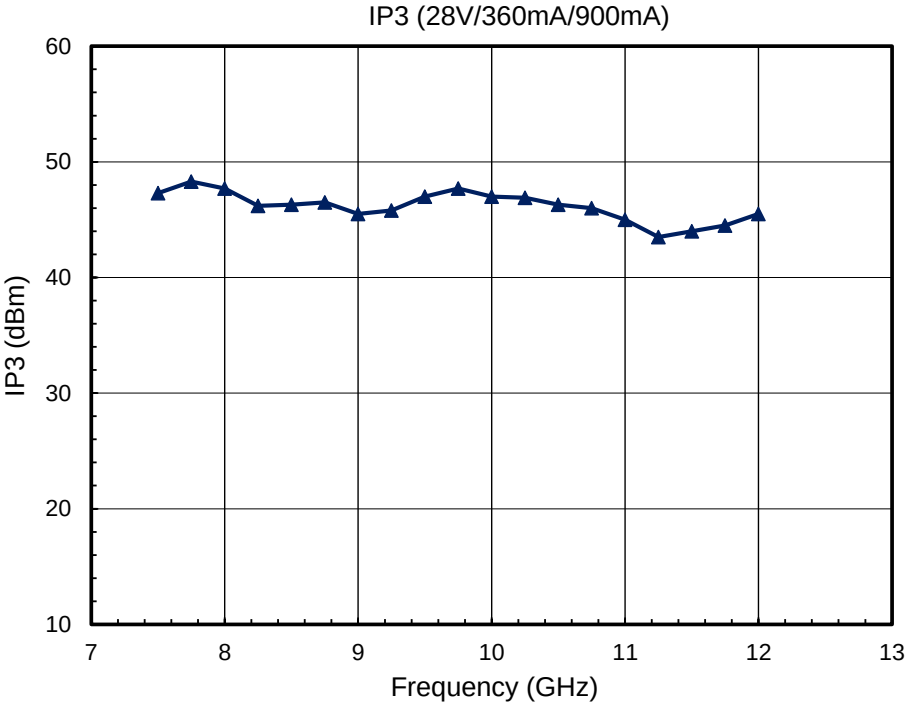
** Power measured using test fixture. Bias is V_{ds1} = V_{ds2} = +15V , I_{ds1} =360mA , I_{ds2}=900mA , V_{gs1} = V_{gs2} =-2.3V . Gain in the two graphs is the compressed gain at 1dB and 5dB compression respectively.



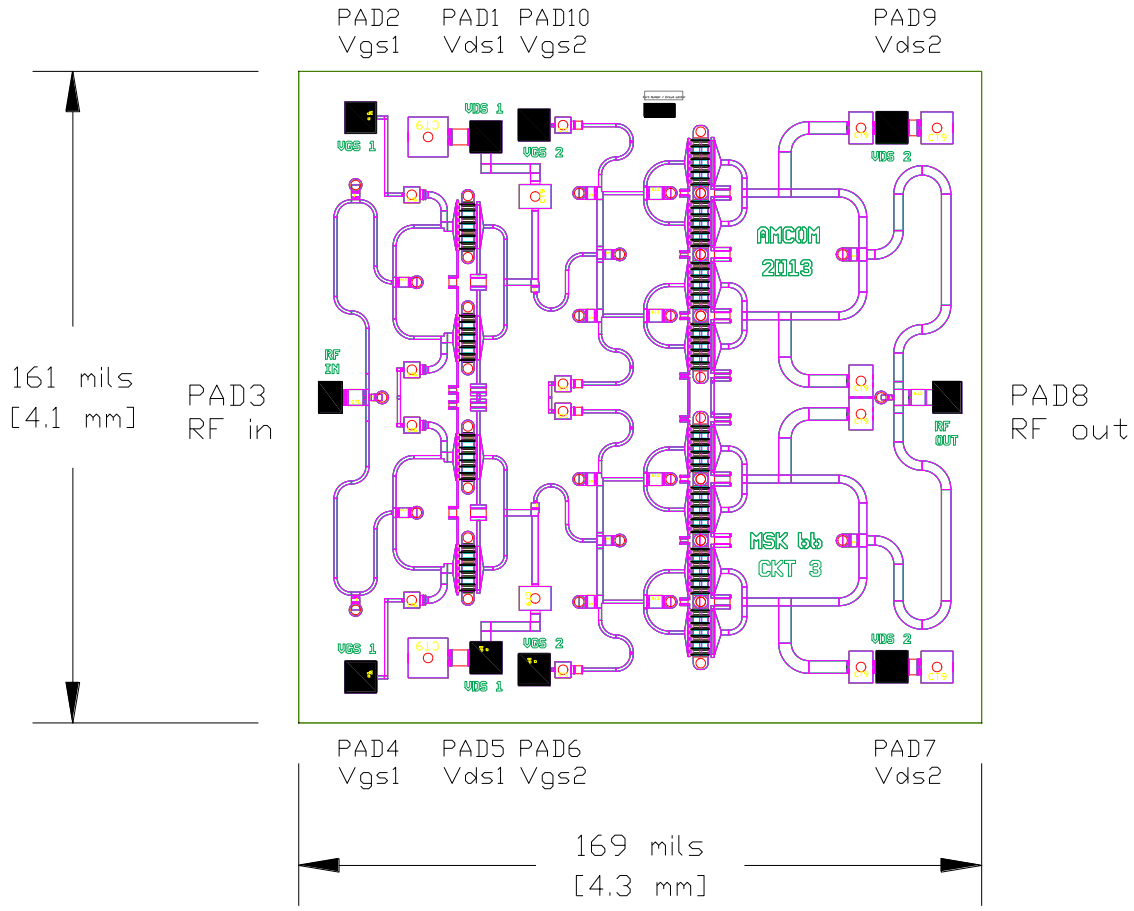


** Power measured using test fixture. Bias is V_{ds1} = V_{ds2} = +28V , I_{ds1} =360mA , I_{ds2}=900mA , V_{gs1} = V_{gs2} =-2.3V . Gain in the two graphs is the compressed gain at 1dB and 5dB compression respectively.


IP3 (15V/360mA/900mA)
IP3 (dBm)
60
50
40
30
20
10
7
8
9
10
11
12
13
Frequency (GHz)


IP3 (28V/360mA/900mA)
IP3 (dBm)
60
50
40
30
20
10
7
8
9
10
11
12
13
Frequency (GHz)

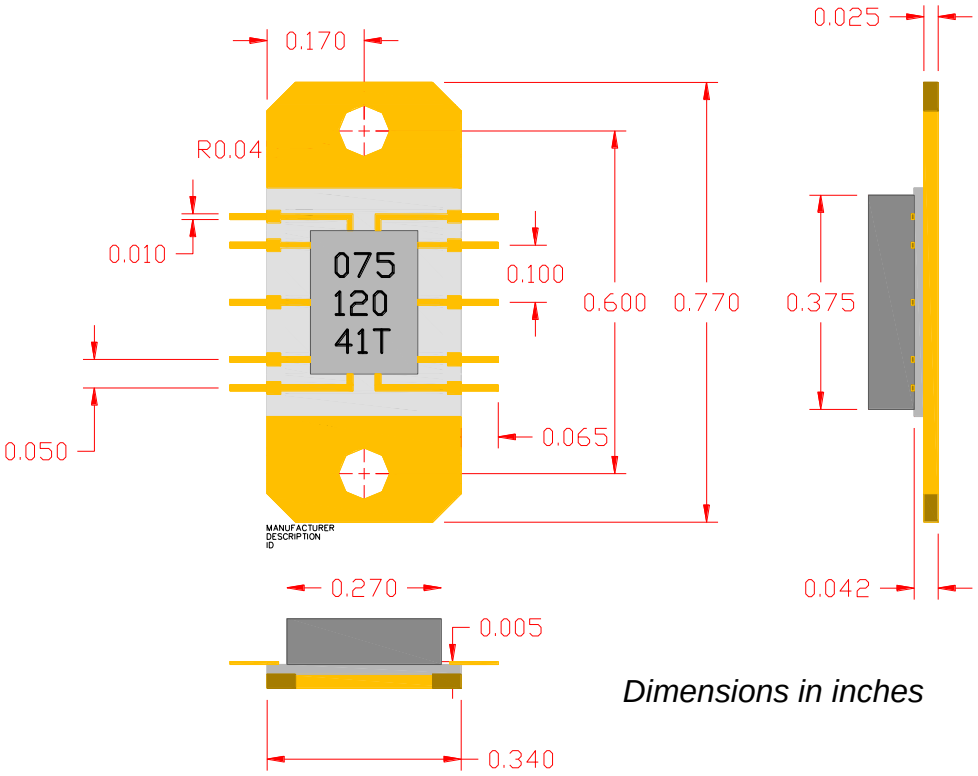
CHIP OUTLINE



NOTES:
1- All PADs are 200 x 200microns
2- Input RF PADs is 150 x 200microns

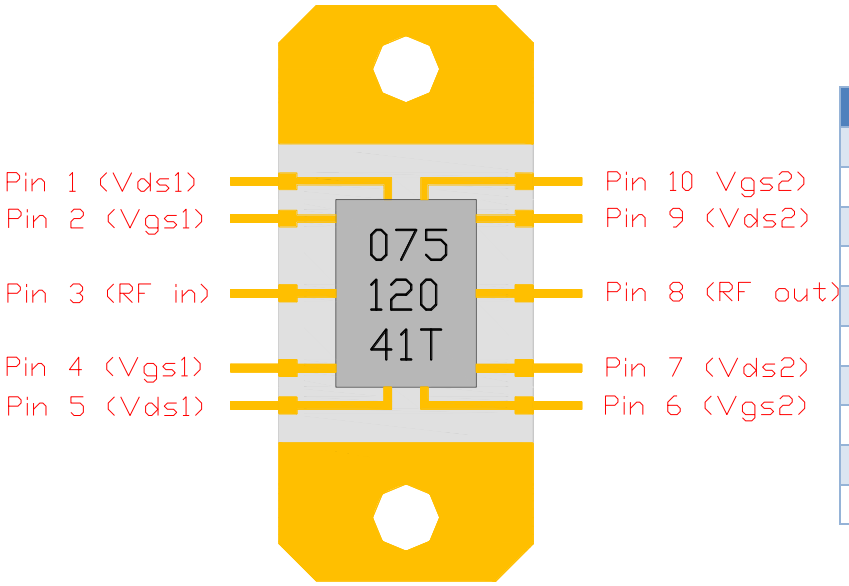
PAD No.	Function	Bias
1	Vds1	+28V
2	Vgs1	-2.3V
3	RF in	-
4	Vgs1	-2.3V
5	Vds1	+28V
6	Vgs2	-2.3V
7	Vds2	+28V
8	RF out	-
9	Vds2	+28V
10	Vgs2	-2.3V

PACKAGE OUTLINE



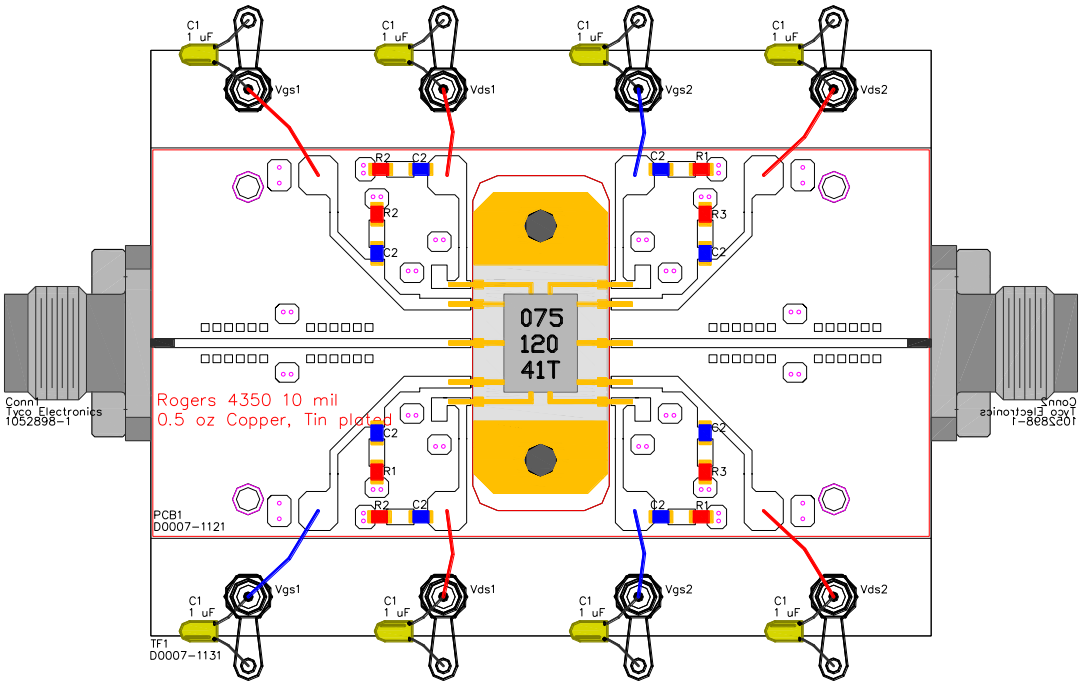
Dimensions in inches

Pin Layout



Pin No.	Function	Bias
1	Vds1	+28V
2	Vgs1	-2.3V
3	RF in	-
4	Vgs1	-2.3V
5	Vds1	+28V
6	Vgs2	-2.3V
7	Vds2	+28V
8	RF out	-
9	Vds2	+28V
10	Vgs2	-2.3V

TEST CIRCUIT



Notes:
1- Use epoxy to mount PCB
2- C1=1uF, C2=1000pF, R1=50ohms, R2=10ohms, R3=5ohms
3- All SMT Caps & Resistors are 0603 size

Important Notes:

1- Recommended current biases are 360mA for the first stage and 900mA for the second stage. Gate biases of -2.3V are for reference only. V_{gs1} & V_{gs2} could be adjusted to vary the currents going thru the first stage (V_{ds1} pins) & second stage (V_{ds2} pins).

2- Do not apply V_{ds1} or V_{ds2} without proper negative voltages on V_{gs1} & V_{gs2}. Otherwise MMIC would fail due to excess current and heat.