

DESCRIPTION

AMCOM's AM003536WM-BM/EM/FM-R is an ultra-broadband GaAs MMIC power amplifier. It has 22 dB gain and 36dBm output power over the 0.01 to 3.5 GHz band. This MMIC is in a ceramic package with both RF and DC leads at the lower level of the package to facilitate low-cost SMT assembly to the PC board. When mounting directly to the PCB, please see application note ANB700 for instructions. Because of high power dissipation, we strongly recommend to mount these devices directly on a metal heat sink. The AM003536WM-EM is a Copper Tungsten drop-in package with straight leads. The AM003536WM-FM-R is the AM003536WM-BM-R mounted on a gold-plated copper flange carrier. There are two screw holes on the flange to facilitate screwing on to a metal heat sink. Both parts are RoHS compliant.

FEATURES

- Wide bandwidth from 10MHz to 3.5 GHz
- High output power, P1dB = 36dBm
- High gain, 22dB
- Input /Output matched to 50 Ohms

APPLICATIONS

- Software Radio
- Instrumentation
- Gain block

TYPICAL PERFORMANCE * (Bias Conditions**: $V_{dd} = +20V$, $I_{dq1} = 125mA$, $I_{dq2} = 550mA$)

Parameters	Minimum	Typical **	Maximum
Frequency	0.02 – 2.5GHz	0.01 – 3.5GHz	-
Small Signal Gain	19 dB	22 dB	26 dB
Gain Ripple	-	± 1.5 dB	± 3.0 dB
P1dB @ 1 GHz	32.5 dBm	34.0 dBm	-
Psat	34.5 dBm	36.0 dBm	-
Efficiency @ P1dB	-	20 %	
IP3 @ 1GHz	-	48 dBm	
Input Return Loss	13 dB	20dB	
Output Return Loss	7 dB	10dB	
Thermal Resistance		4.5 °C/W	

* Specifications subject to change without notice.

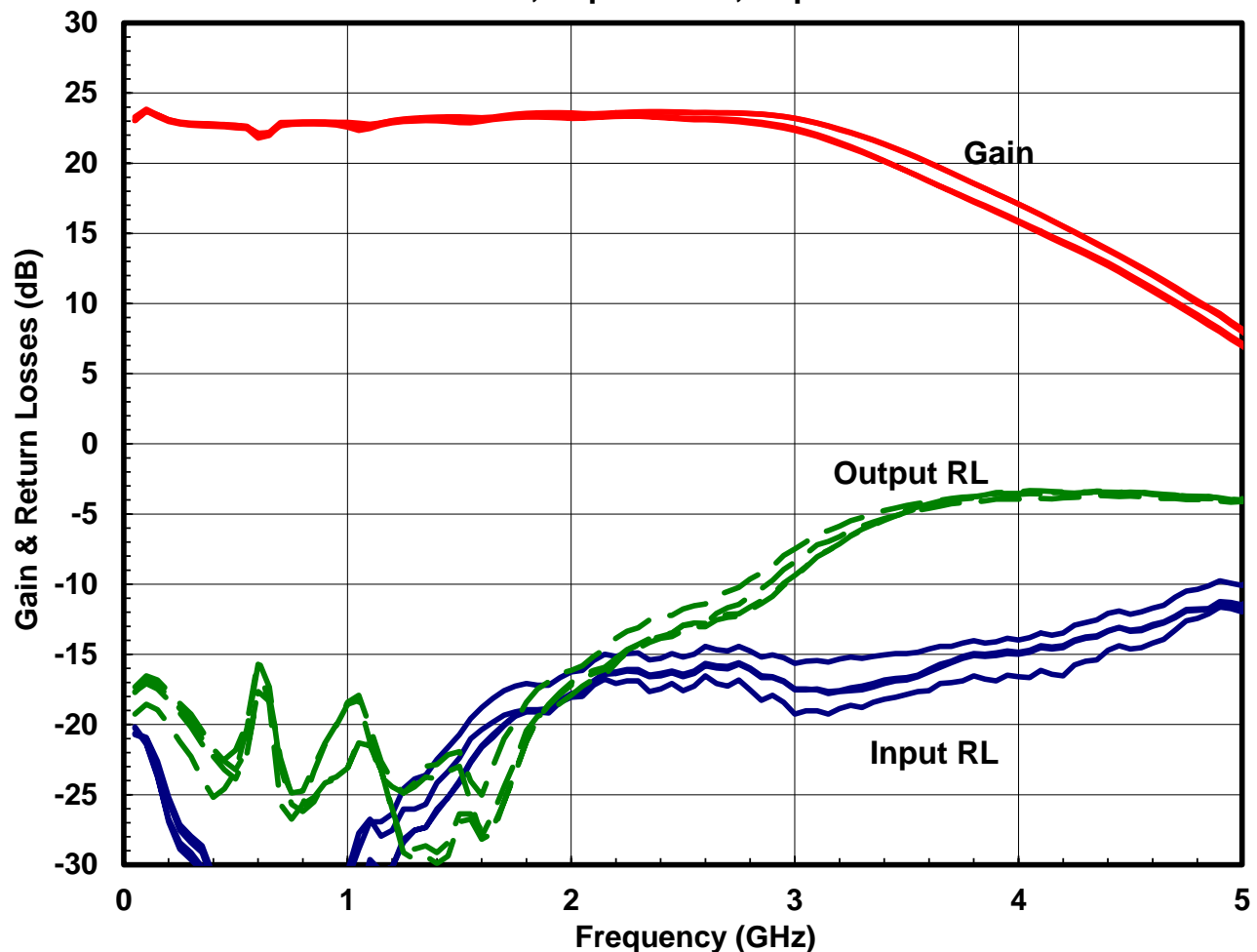
** Gate biases corresponding to above currents are $V_{gs1} = -1.2V$, $I_{gs1} < 2mA$, $V_{gs2} = -0.8V$, $I_{gs2} < 5mA$ and may vary from lot to lot. Gate currents could reach above limits only near power saturation

ABSOLUTE MAXIMUM RATING

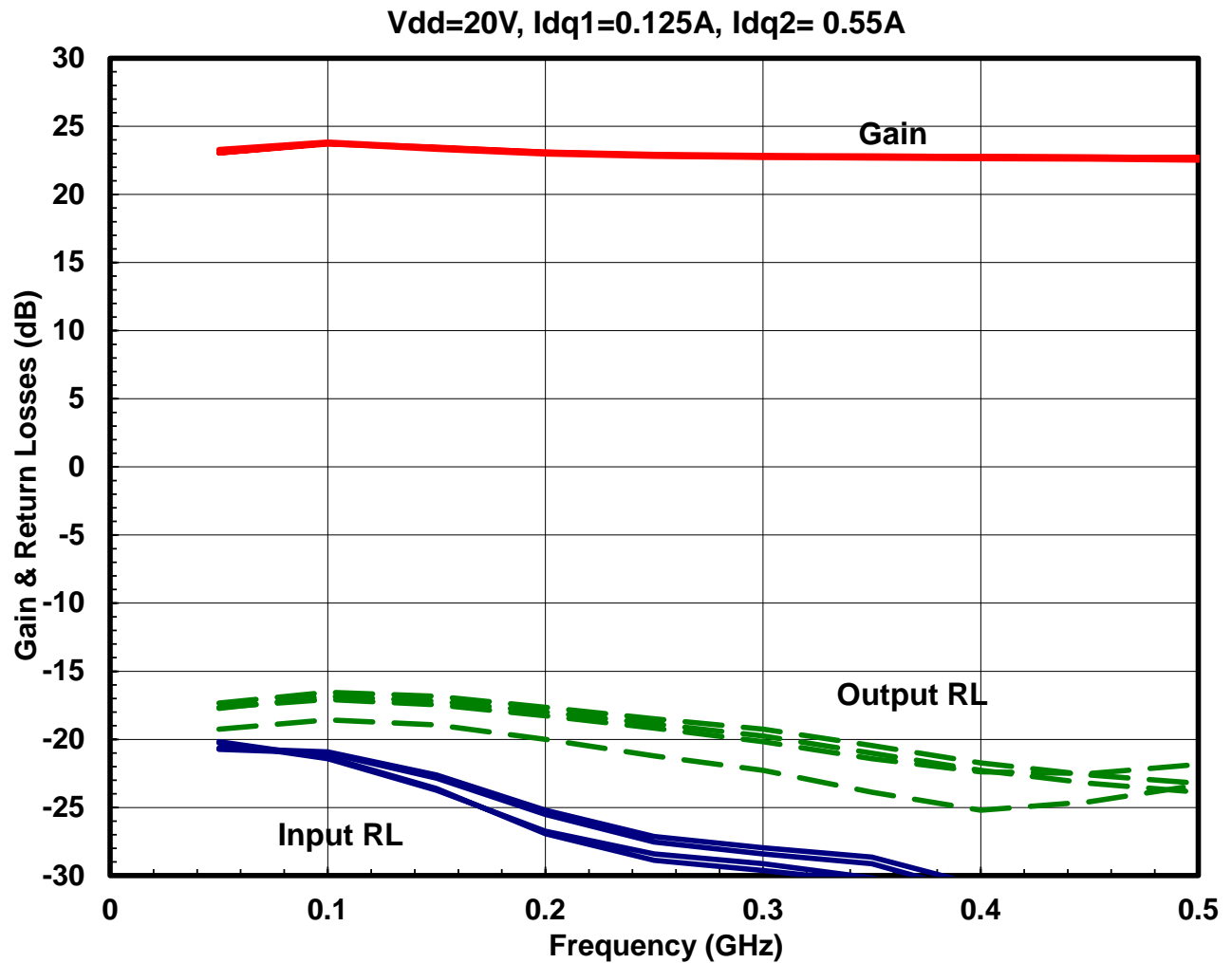
Parameter	Symbol	Rating
Drain source voltage	V_{dd}	24 V
Gate source voltage	V_{gs1} & V_{gs2}	-3 V
Drain source current	I_{dq1}	150 mA
Drain source current	I_{dq2}	600 mA
Continuous dissipation at 25°C	P_t	18 W
Channel temperature	T_{ch}	175 °C
Operating temperature	T_{op}	-55°C to +85°C
Storage temperature	T_{sto}	-55°C to +135°C
Input power	P_{in}	18dBm

SMALL SIGNAL DATA*

$V_{dd}=20V, I_{dq1}=0.125A, I_{dq2}= 0.55A$

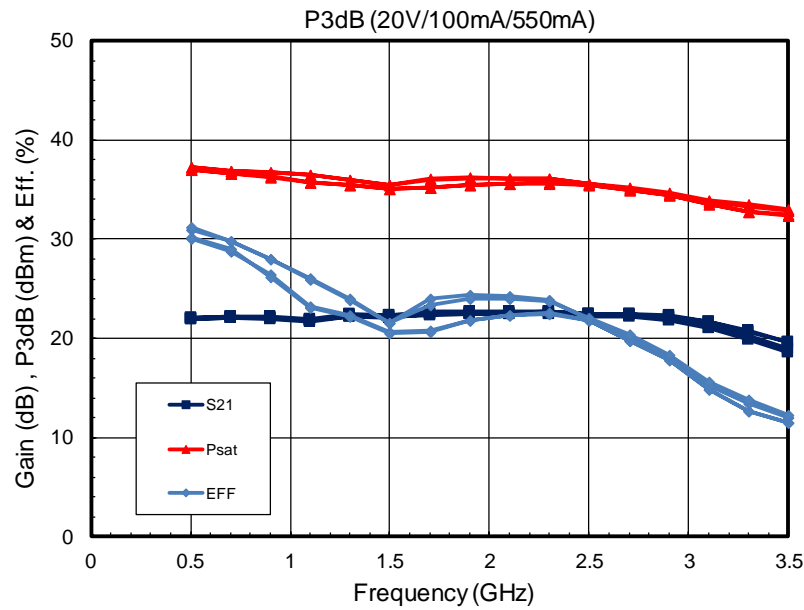
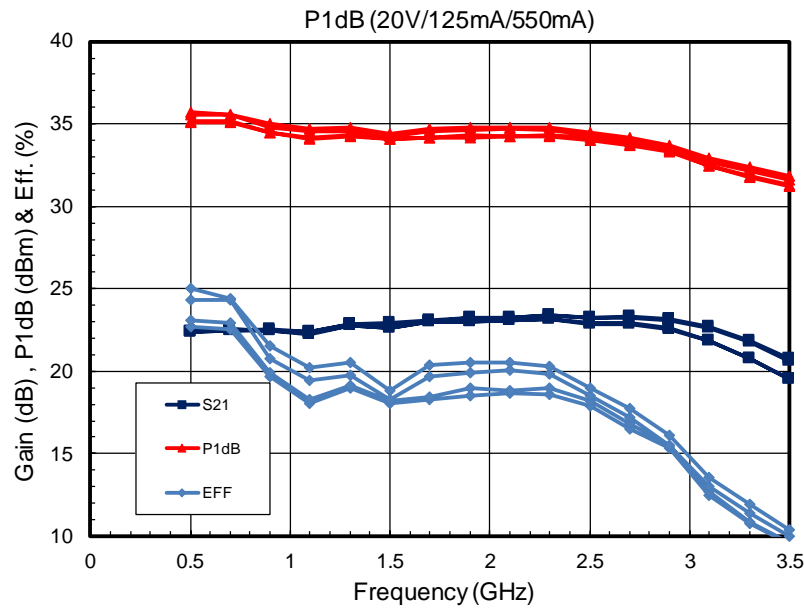


EXTENDED LOW FREQUENCY SCALE



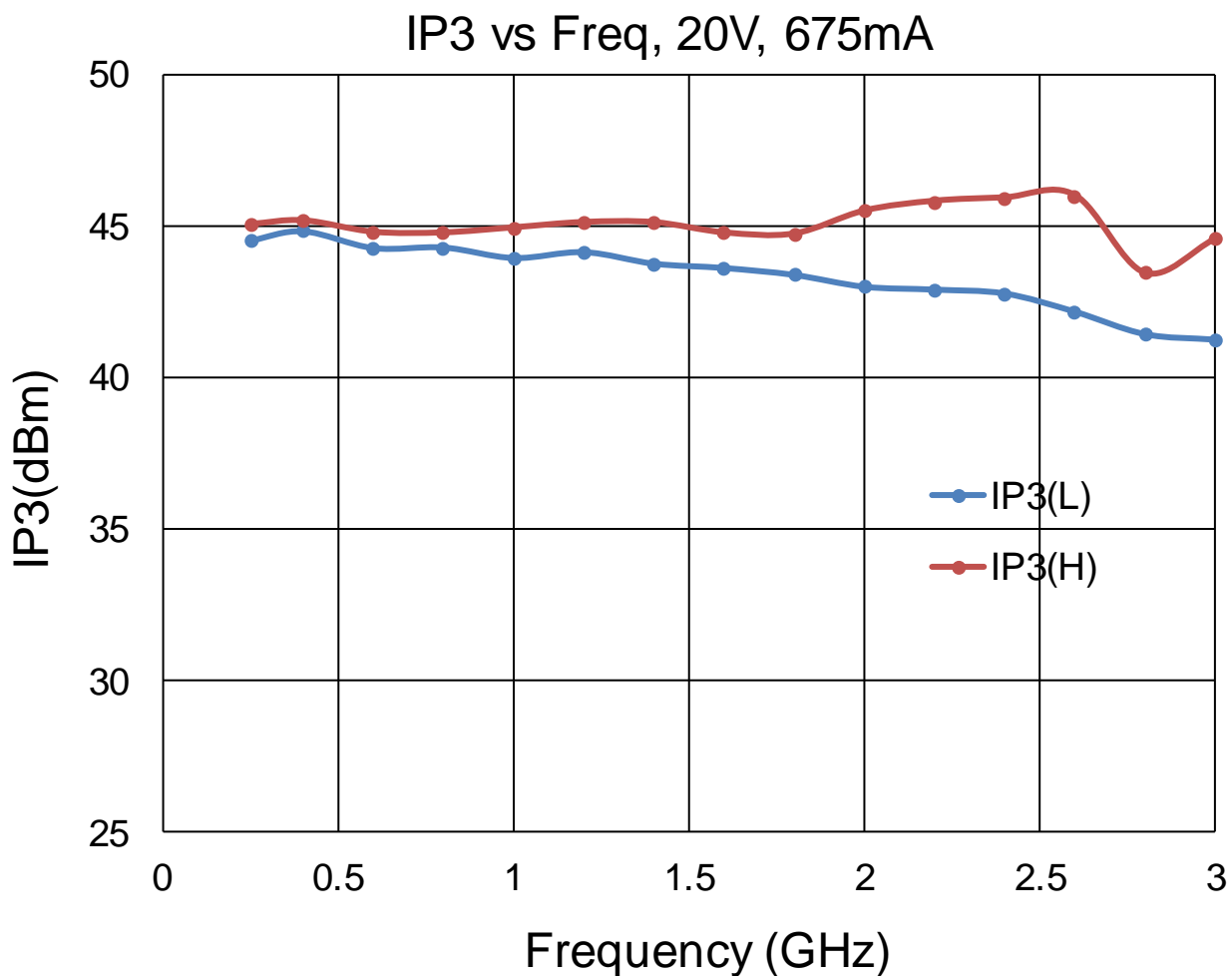
* S-Parameters measured using bias tee at the output. MMIC could be operated at lower than $V_{dd}=+20V$ with almost same small signal parameters. V_{gs1} & V_{gs2} vary with V_{dd} and may need slight adjustments

POWER DATA*

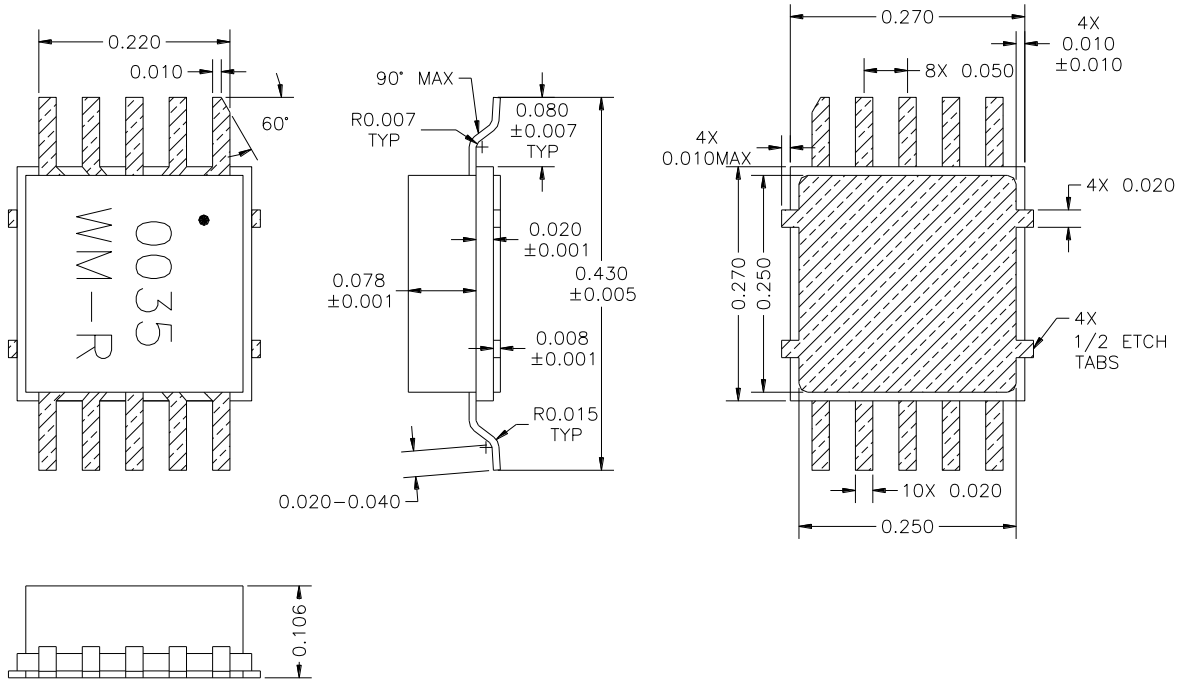


* Power measured using bias tee at the output. MMIC could be operated at lower than $V_{dd}=+20V$ with reduced power output. V_{gs1} & V_{gs2} vary with V_{dd} and may need slight adjustments

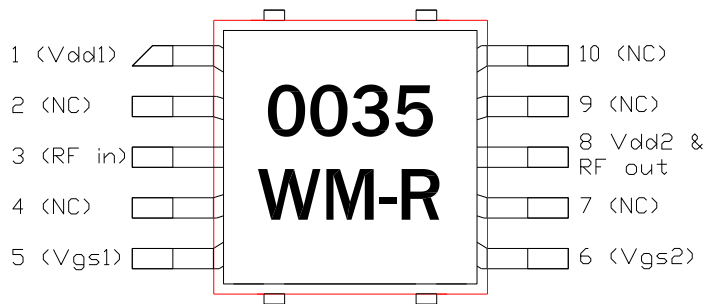
THIRD ORDER INTERCEPT



PACKAGE OUTLINE (BM)



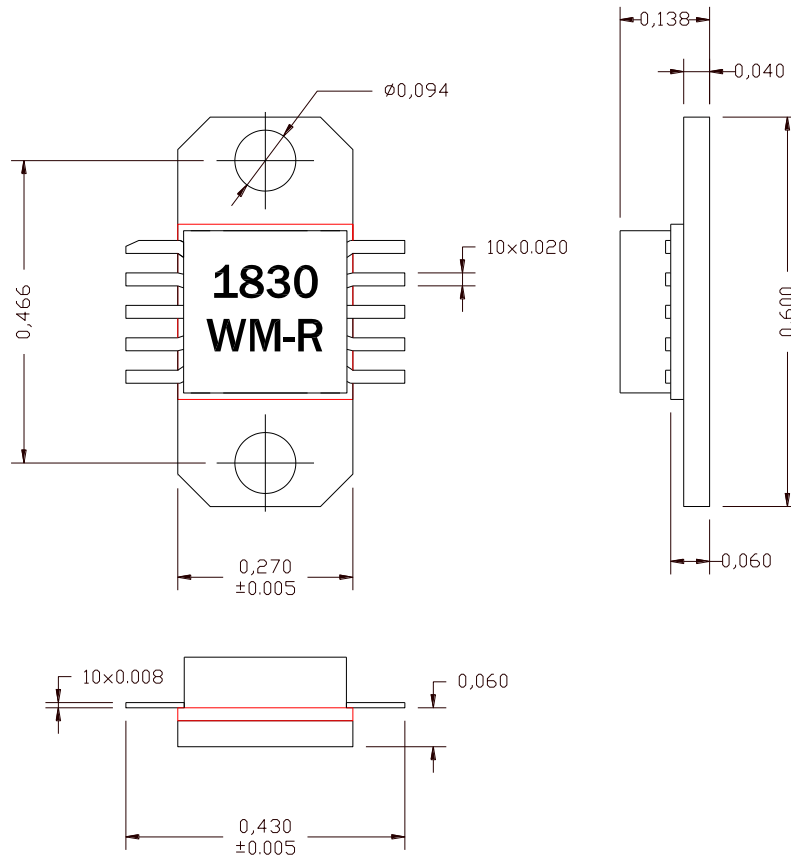
PIN LAYOUT



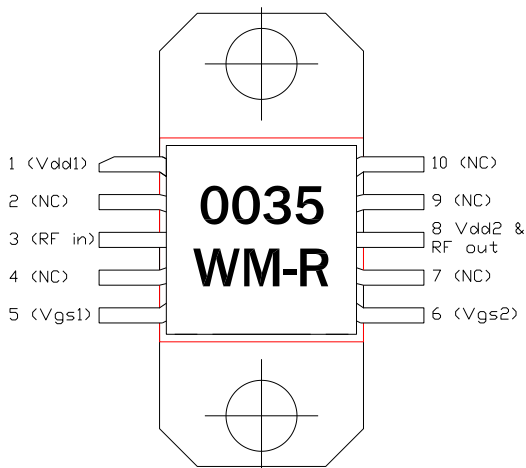
Pin No.	Function	Bias*
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-1.2V
6	Vgs2	-0.8V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

* Gate biases are for reference only and may vary from lot to lot

PACKAGE OUTLINE (EM)



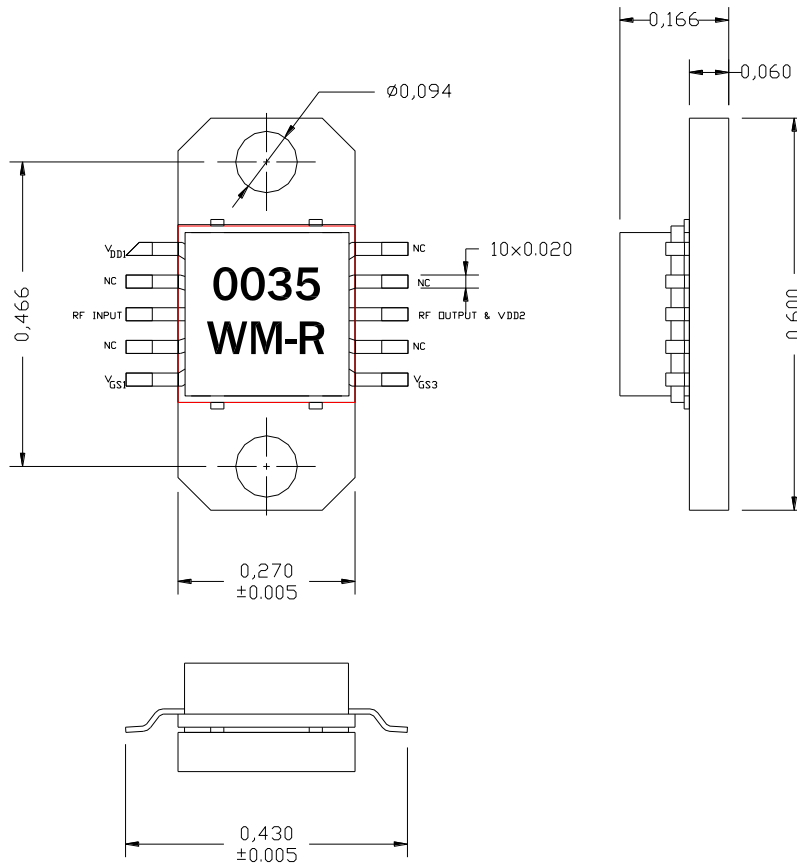
PIN LAYOUT



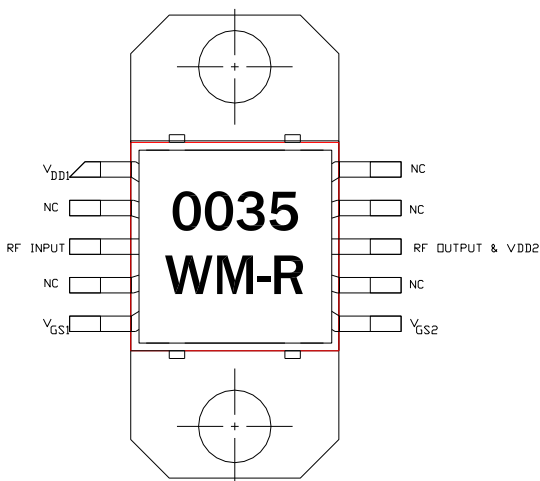
Pin No.	Function	Bias*
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-1.2V
6	Vgs2	-0.8V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

* Gate voltage may vary from lot to lot

PACKAGE OUTLINE (FM)



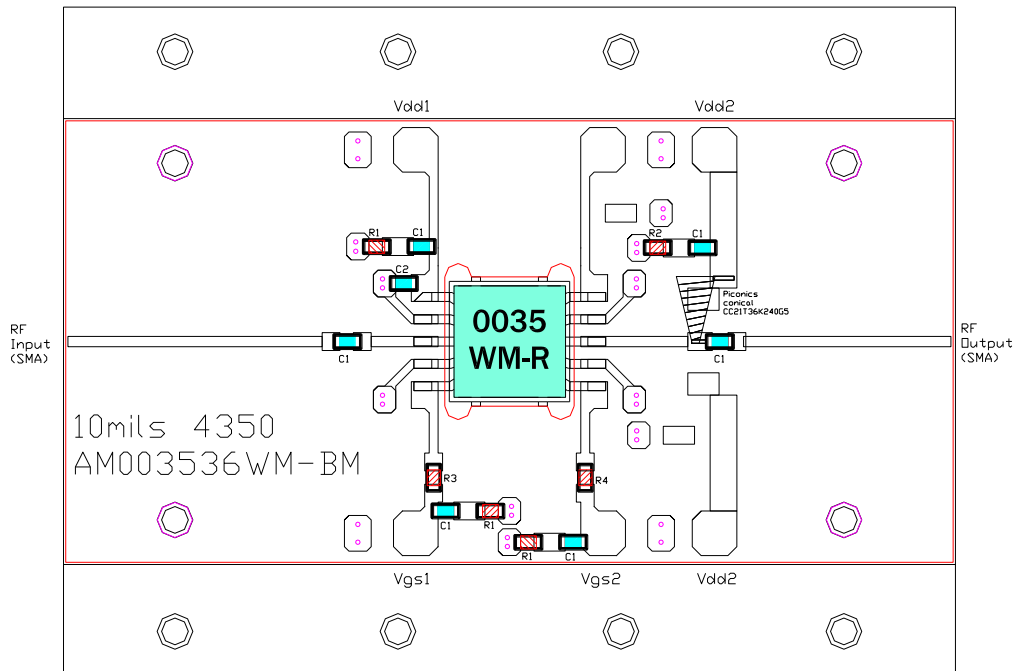
PIN LAYOUT



Pin No.	Function	Bias*
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-1.2V
6	Vgs2	-0.8V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

* Gate voltage may vary from lot to lot

TEST CIRCUIT for BM Package



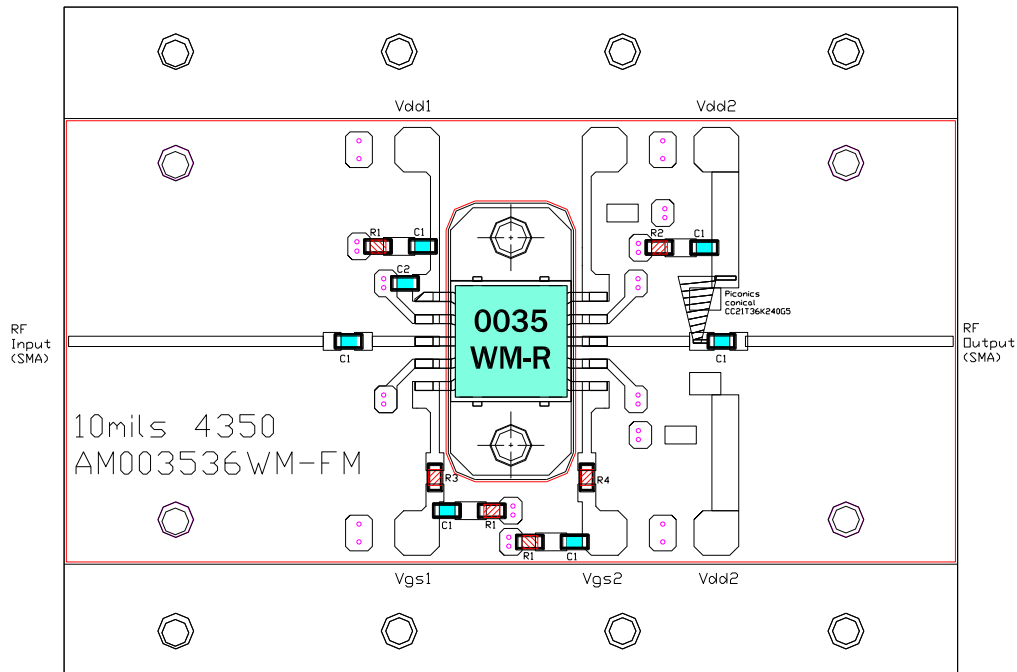
Notes:

- 1- 10mils Rogers 4350 Material epoxied to TF
- 2- Ckt is for AM003536WM-BM, AM012535MM-BM & AM002535MM-BM
- 3- C1=1000pF, C2=20pF,
R1=50 Ohms, R2=10 ohms, R3=1000 Ohms, R4=500 Ohms
- 4- All Caps & Resistors are 0603 size

Important Notes:

- 1- The +20V Bias to the output port could be provided via a bias tee or suitable chokes to be soldered on the board. Inductance of choke should be large enough to have high impedance at lowest frequency of operation (300nH is adequate).
- 2- Recommended current biases are 125mA and 500mA for the first stage and second stage respectively. At V_{dd1} & $V_{dd2} = +20V$, V_{gs1} & V_{gs2} values are -1.2V and -0.80V respectively to obtain these desired currents. V_{gs1} & V_{gs2} could be adjusted to vary the currents going thru the first stage (V_{dd1} pin) and the second stage (V_{dd2} pin) respectively. Gate biases are for reference only.
- 3- Do not apply V_{dd1} & V_{dd2} without proper negative voltages on V_{gs1} & V_{gs2} .
- 4- The currents flowing out of the V_{gs1} & V_{gs2} pins are less than 2mA & 5mA respectively at P_{1dB} .
- 5- DC blocking capacitors must be used at input and output.

TEST CIRCUIT for EM & FM Package



Notes:

- 1- 10mils Rogers 4350 Material epoxied to TF
- 2- Ckt is for AM003536WM-FM , AM012535MM-FM & AM002535MM-FM
- 3- C1=1000pF, C2=20pF,
R1=50 Ohms, R2=10 ohms, R3=1000 Ohms, R4=500 Ohms
- 4- All Caps & Resistors are 0603 size

Important Notes:

- 1- The +20V Bias to the output port could be provided via a bias tee or suitable chokes to be soldered on the board. Inductance of choke should be large enough to have high impedance at lowest frequency of operation (300nH is adequate).
- 2- Recommended current biases are 125mA and 500mA for the first stage and second stage respectively. At V_{dd1} & $V_{dd2} = +20V$, V_{gs1} & V_{gs2} values are -1.2V and -0.80V respectively to obtain these desired currents. V_{gs1} & V_{gs2} could be adjusted to vary the currents going thru the first stage (V_{dd1} pin) and the second stage (V_{dd2} pin) respectively. Gate biases are for reference only.
- 3- Do not apply V_{dd1} & V_{dd2} without proper negative voltages on V_{gs1} & V_{gs2} .
- 4- The currents flowing out of the V_{gs1} & V_{gs2} pins are less than 2mA & 5mA respectively at P_{1dB} .
- 5- DC blocking capacitors must be used at input and output.